IF YOU CANNOT FIND THE

SIGNETICS MEMORY PART

THAT YOU REQUIRE -

WHY NOT TRY OUR

BIPOLAR and MOS

ROMS and RAMS

SIGNETICS MEMORY SELECTION GUIDE PAGES (iv) & (v)

OR ASK FOR OUR

MOS AND BIPOLAR MEMORY BOOKLET

STATIC SHIFT REGISTERS

Part Number	Capacity	Output Structure	On Chip Re-Circulate	Package No. of Leads	TYP Speed	Number of Clocks	Clock TTL Compati-bility	Power Supplies	Page No.
2533	1024 BITS	Push Pull	JUMPER	V-8	2.0 MHz	ONE	YES	+5, -12	49
2527	Dual 256 BITS	Push Pull	YES	V-8	3.0 MHz	ONE	YES	+5, -12	39
2528	Dual 250 BITS	Push Pull	YES	V-8	3.0 MHz	ONE	YES	+5, -12	39
2529	Dual 240 BITS	Push Pull	YES	V-8	3.0 MHz	ONE	YES	+5, -12	29
2511	Dual 200 BITS	Tri-state	YES	A-14, K-10	3.0 MHz	ONE	YES	+5, -5, -12	17
2522	Dual 132 BITS	Push Pull	YES	V-8	3.0 MHz	ONE	YES	+5, -12	29
2521	Dual 128 BITS	Push Pull	YES	V-8	3.0 MHz	ONE	YES	+5, -12	29
2510	Dual 100 BITS	Tri-state	YES	A-14, K-10	3.0 MHz	ONE	YES	+5, -5, -12	17
2532	Quad 80 BITS	Push Pull	YES	B-16	3.0 MHz	ONE	YES	+5, -12	45
2509	Dual 50 BITS	Tri-state	YES	A-14, K-10	3.0 MHz	ONE	YES	+5, -5, -12	17
2519	Hex 40 BITS	Bare Drain	YES	B-16	3.0 MHz	ONE	YES	+5, -12	24
2518	Hex 32 BITS	Bare Drain	YES	B-16	3.0 MHz	ONE	YES	+5, -12	24

DYNAMIC SHIFT REGISTERS

Part Number	Capacity	Output Structure	On Chip Re-Circulate	Package No. of Leads	TYP Speed	Number of Clocks	Clock TTL Compati-bility	Power Supplies	Page No.
2504	1024 BITS	Bare Drain	NO	TA-8, V-8	10.0 MHz	TWO	NO	+5, -5	1
2512	1024 BITS	Bare Drain	YES	K-10	3.0 MHz	TWO	NO	+5, -5	6
2525	1024 BITS	Bare Drain	YES	V-8	5.0 MHz	TWO	NO	+5, -5	34
2503	Dual 512 BITS	Bare Drain	NO	TA-8, V-8	10.0 MHz	TWO	NO	+5, -5	1
2505	512 BITS	Bare Drain	YES	K-10	3.0 MHz	TWO	NO	+5, -5	6
2524	512 BITS	Bare Drain	YES	V-8	5.0 MHz	TWO	NO	+5, -5	34
2502	Quad 256 BITS	Bare Drain	NO	B-16	10.0 MHz	TWO	NO	+5, -5	1
2506	Dual 100 BITS	Bare Drain	NO	T-8, V-8	4.0 MHz	TWO	NO	+5, -5	12
2507	Dual 100 BITS	7.5K PD	NO	T-8, V-8	4.0 MHz	TWO	NO	+5, -5	12
2517	Dual 100 BITS	20K PD	NO	T-8, V-8	4.0 MHz	TWO	NO	+5, -5	12

MOS MEMORY SELECTION GUIDE

Micropressor 8-bit Signetics 2650

Type	Org.	Max. Access Time (ns)	Signetics Part No.
ROM	64x8x5	600	2513
	64x6x8	600	2516
	64x9x9	700	2526
	512x8	700	2530
	2048x4	950	2580
	1024x8	400	2608
RAM	256x1	1000	2501
		1000	25L01
	1024x1	300	1103
		150	1103-1
		1000	2602/2102
		500	2602-1/2102-1
		650	2602-2/2102-2
		350	21F02
		250	21F02-2
		450	21F02-4
		1000	21L02
		500	21L02-1
		650	21L02-2
		400	21L02-3
		450	M2102-4
		650	M2102-6
	256x4	750	2606
		500	2606-1
	4096x1	300	2604
		300	2660
		200	2670
		200	2680

BIPOLAR MEMORY SELECTION GUIDE

	Type	Configuration	Output	Signetics Part No.
TTL	ROM	256x4	OC TS	82S226 82S229
		512x4	OC TS	82S230 82S231
		256x8	TS	8204/S214
		512x8	TS	8205/S215
		1024x4	TTL	8228
	PROM	32x8	OC TS	82S23 82S123
		256x4	OC TS	82S126 82S129
		512x4	OC TS	82S130 82S131
		256x8	TS	82S114
		512x8	TS	82S115
	FPLA	16x48x8	TS OC	82S100 82S101
ECL	PROM	32x8	OE	10139
		256x4	OE	10149

OC = Open Collector
TS = Tri-State
TTL = Totem Pole
OE = Open Emitter

	Type	Org.	Output	Signetics Part No.
TTL	RAM	16x4	OC (B) OC (NB)	82S25/3101A 74S89
		256	TS (NB) TS (B) OC (NB) OC (B)	82S16/82S116 74S200/201 82S17/117 74S301
		64x9	OC	82S09
		1024x1	OC (B) TS (B)	82S10 82S11
	CAM	4x2	OC	8220
	WWR	32x2	OC	82S21
	SAM	8x4	OC TS	82S12 82S112
	RAM	64x1	OE	10140/10148
ECL		16x4	OE	10145
		256x1	OE	10144
		1024x1	OE	10146
	WWR	64x1	OE	10151
	CAM	8x2	OE	10155

OC = Open Collector
TS = Tri-State
OE = Open Emitter
(B) = O/P Blanked During Write
(NB) = O/P Non-Blanked During Write

signetics

1024-BIT CAPACITY MULTIPLEXED DYNAMIC SHIFT REGISTERS

SILICON GATE MOS 2500 SERIES

2502
2503
2504

DESCRIPTION

These Signetics 2500 Series 1024-bit multiplexed dynamic shift registers consist of enhancement mode P-channel MOS devices integrated on a single monolithic chip. Due to on-chip multiplexing, the data rate is twice the clock rate.

FEATURES

- 10 MHz TYPICAL DATA RATE
- THREE CONFIGURATIONS—QUAD 256, DUAL 512, SINGLE 1024
- LOW POWER DISSIPATION: 40 μW/BIT AT 1 MHz DATA RATE
- TTL, DTL COMPATIBLE
- STANDARD PACKAGES
- SIGNETICS P-MOS SILICON GATE PROCESS AND SILICONE PACKAGING TECHNOLOGIES

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST BUFFER MEMORIES
CRT REFRESH MEMORIES
DELAY LINE MEMORY REPLACEMENT

PROCESS TECHNOLOGY

Use of low threshold *silicon gate technology* allows high speed (10 MHz typical) while reducing power dissipation and clock input capacitance dramatically as compared to metal gate technologies.

The use of low voltage circuitry minimizes power dissipation and facilitates interfacing with bipolar integrated circuits.

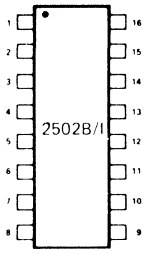
SILICONE PACKAGING

Low cost silicone DIP packaging is implemented, and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process, the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric material over the silicon gate-oxide-substrate structure provides an ion barrier. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability and demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers.

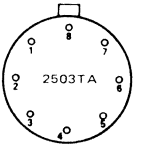
BIPOLAR COMPATIBILITY

The data inputs of these registers can be driven directly by standard bipolar integrated (TTL, DTL, etc.) or by MOS circuits. The bare drain output stage provides driving capability for both MOS and bipolar integrated circuits (one standard TTL load).

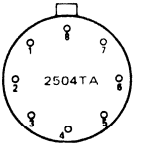
PIN CONFIGURATIONS (Top View)



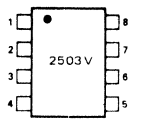
1.	OUT 1	16.	IN 4
2.	NC	15.	NC
3.	IN 1	14.	OUT 4
4.	ϕ1	13.	NC
5.	V_{CC}	12.	V_{DD}
6.	OUT 2	11.	ϕ2
7.	NC	10.	IN 3
8.	IN 2	9.	OUT 3



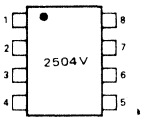
1.	OUT 1	5.	OUT 2
2.	IN 1	6.	IN 2
3.	ϕ1	7.	ϕ2
4.	V_{CC}	8.	V_{DD}



1.	NC	5.	OUT
2.	IN	6.	NC
3.	ϕ1	7.	ϕ2
4.	V_{CC}	8.	V_{DD}



1.	OUT_2	8.	V_{CC}
2.	IN_2	7.	ϕ_1
3.	ϕ_2	6.	IN_1
4.	V_{DD}	5.	OUT_1



1.	OUT	8.	V_{CC}
2.	ϕ_2	7.	NC
3.	NC	6.	ϕ_1
4.	V_{DD}	5.	IN

PART IDENTIFICATION TABLE

TYPE	FUNCTION	PACKAGE
2502B	Quad 256-bit	16-Pin Silicone DIP
2502I	Quad 256-bit	16-Pin Ceramic DIP
2503TA	Dual 512-bit	TO-99
2503V	Dual 512-bit	8-Pin DIP
2504TA	Single 1024-bit	TO-99
2504V	Single 1024-bit	8-Pin DIP

MAXIMUM SIGNETICS GUARANTEED RATINGS(1)

Operating Ambient Temperature(2)	0°C to +70°C
Storage Temperature	-65°C to + 150°C
Power Dissipation(2) at T_A = 70°C	
TA and V Package	535mW
B Package	640mW
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}(3)	+0.3V to -20V

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W (TA and V package)or 125° C/W (B package).
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserving the right to make design and process changes and improvements.
7. Typical values at +25°C and nominal supply voltages.
8. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are $V_{IH} = V_{CC} - 1.85V$ and $V_{IL} = V_{CC} - 4.15V$.
9. When cascading use 140nc minimum pulse width to allow data set-up time for driver register.

DC CHARACTERISTICS

T_A = 0°C to +70°C; V_{DD} = -5V ±5%; V_{CC} = +5V(8) unless otherwise noted. (See Notes 4,5,6,7).

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	$V_{IN} = V_{CC}$ to V_{DD}, T_A = 25°C
I_{LO}	Output Leakage Current		10	1000	nA	$V_{\phi1} = V_{\phi2} = -10V$ V_{OUT} = 0.0V, T_A = 25°C
I_{LC}	Clock Leakage Current		10	1000	nA	V_{ILC} = −10V , T_A = 25°C
I_{DD}	Power Supply Current		15	25	mA	Outputs at logic "0", 4 MHz data rate, $\phi1 = \phi2$ = 85ns continuous operation, V_{ILC} = −12V T_A = 25°C
V_{IL}	Input "Low" Voltage			+0.6	V	See Note 8
V_{IH}	Input "High" Voltage	+3.4		5.3	V	See Note 8
V_{IHC}	Clock Input "High" Voltage	4.0		5.3	V	
V_{ILC}	Clock Input "Low" Voltage	−10		−12	V	

AC CHARACTERISTICS

$T_A = 25°C$, $V_{DD} = -5V \pm 5\%$; $V_{CC} = +5V$ (8) ; $V_{ILC} = -11V$, (See notes 4, 5, 6, 7).

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
Frequency	Clock Rep Rate	0.0005		4	MHz	
Frequency	Data Rep Rate	0.001		8	MHz	
ϕ pw	Clock Pulse Width (9)	85			ns	See note 9
ϕ d	Clock Pulse Delay	10			ns	
t_r, t_f	Clock Pulse Transition	10		1000	ns	
t_w	Data Write Time (Setup)	50			ns	
t_{DO}	Data in Overlap	10			ns	
t_a+	Data Out			90	ns	
C_{IN}	Input Capacitance	2.5		5	pF	@ 1 MHz 25 mV p-p
C_{OUT}	Output Capacitance	2.5		5	pF	@ 1 MHz 25 mV p-p
$C\phi$	Clock Capacitance	130		150	pF	@ 1 MHz 25 mV p-p
V_{OL}	Output "Low" Voltage		-0.3		V	R_L=3k, depends on R_L and TTL Gate
V_{OH1}	Output "High" Voltage Driving MOS	3.6	4.0		V	R_L = 5.6k
V_{OH2}	Output "High" Voltage Driving TTL	3.0	3.5		V	R_L = 3k

MULTIPLEXED 4-BIT MOS SHIFT REGISTER

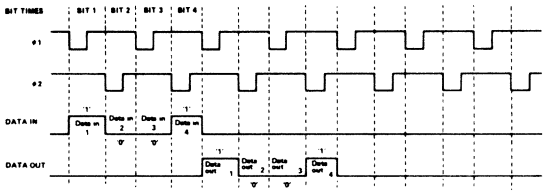


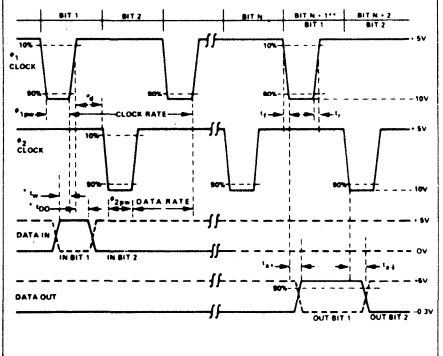
Figure 1

Figure 1 is a simplified illustration of the timing of a 4 bit multiplexed register showing input output relationships with respect to the clock. If data enters the register at $\phi 1$ time, it exits at $\phi 1$ time, (beginning on $\phi 1$'s negative going edge and ending on the succeeding $\phi 2$'s negative going edge).

CONDITIONS OF TEST

Input rise and fall times: 10nsec. Output load is 1 TTL gate.

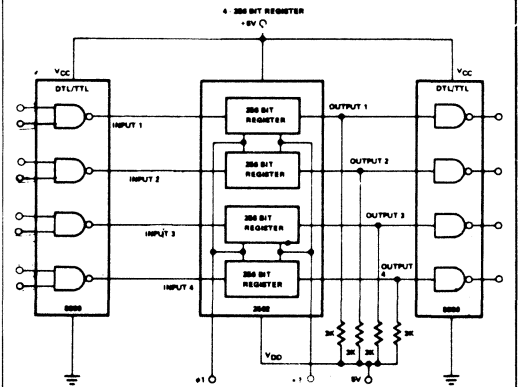
TIMING DIAGRAM



*t_W and t_{DO} same for $\phi 2$
**N=256 for 2502, N = 512 for 2503, N = 1024 for 2504

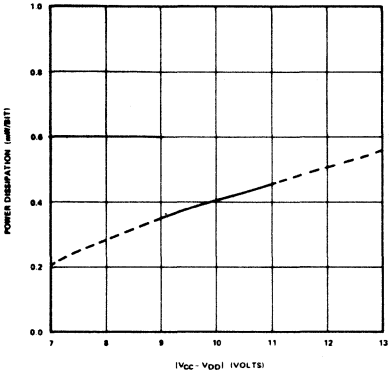
APPLICATIONS INFORMATION

DTL/TTL/MOS INTERFACES

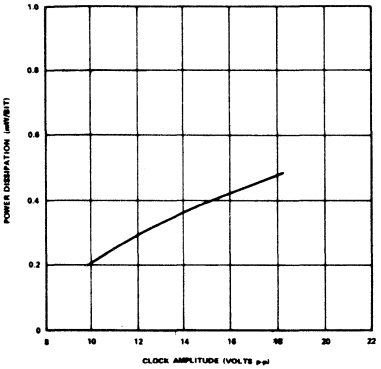


NOTE: When interfacing MOS to MOS output resistors should be 4.7K min

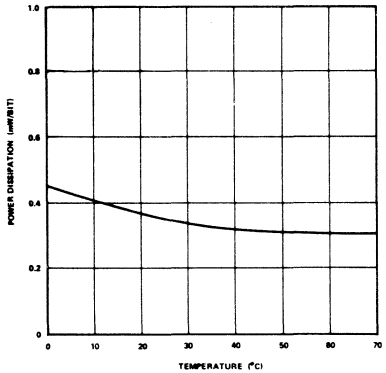
POWER DISSIPATION/BIT VERSUS SUPPLY VOLTAGE



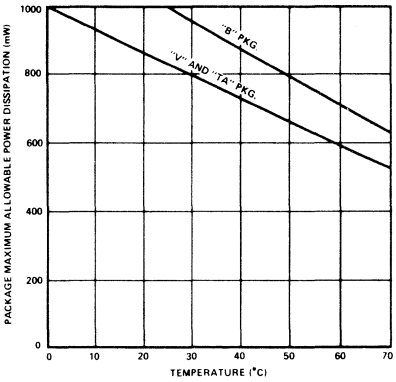
POWER DISSIPATION/BIT VERSUS CLOCK AMPLITUDE



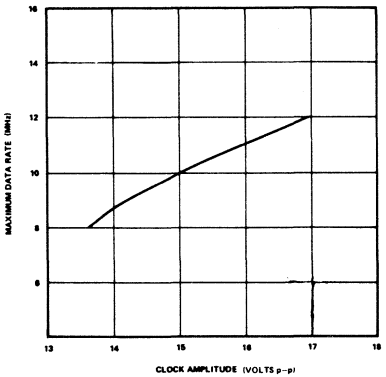
POWER DISSIPATION/BIT VERSUS TEMPERATURE



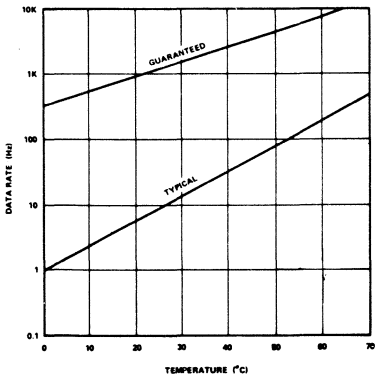
MAXIMUM ALLOWABLE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



CLOCK AMPLITUDE V_ϕ VERSUS MAXIMUM DATA RATE



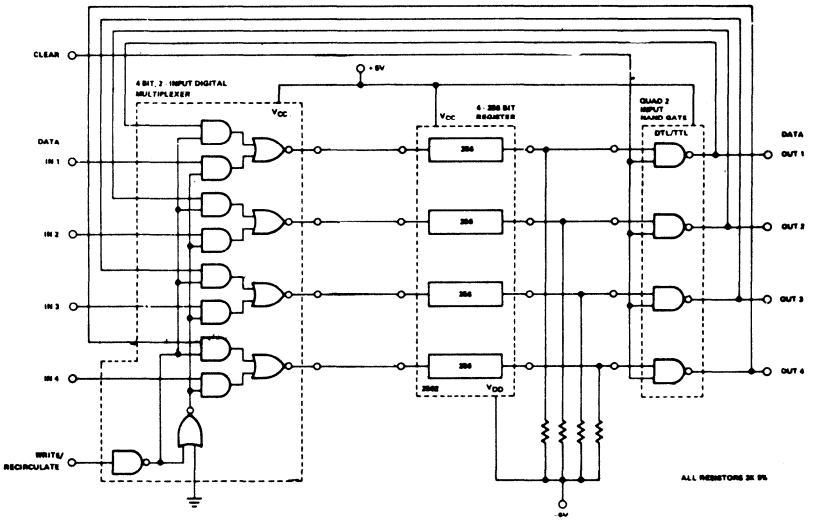
MINIMUM OPERATING DATA RATE VERSUS TEMPERATURE



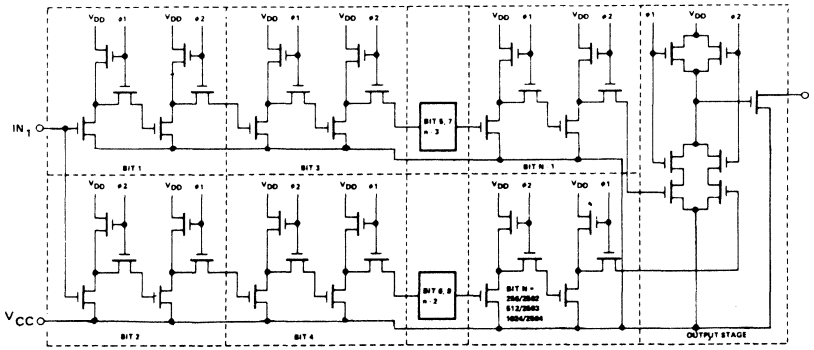
NOTE:
Conditions for Typical Curves; V_{CC} = +5V, V_{DD} = -5V, ϕ_{1PW} and ϕ_{2PW} = 85ns, V_ϕ = -11V, T_A = 25°C, f_{DATA} = 10MHz unless otherwise noted.

APPLICATIONS (Cont'd)

WRITE/RECIRCULATE LOGIC



CIRCUIT SCHEMATIC



NOTES:

1. N = 1024 on 2504
2. N = 512 on 2503 schematic for second register same as above.
3. N = 256 on 2502 schematic for second, third and fourth registers same as above.

signetics

512 AND 1024-BIT RECIRCULATING DYNAMIC SHIFT REGISTERS

2505
2512

SILICON GATE MOS 2500 SERIES

DESCRIPTION

These Signetics 2500 Series 512 and 1024 bit recirculating dynamic shift registers consist of enhancement mode P-channel MOS devices integrated on a single monolithic chip. Internal recirculation logic plus write and read controls, together with two chip select controls are included on the chip.

FEATURES

- HIGH FREQUENCY OPERATION–3 MHz TYPICAL CLOCK RATE
- SINGLE 512, SINGLE 1024
- TTL, DTL COMPATIBLE
- 2-CHIP SELECT CONTROLS FOR XY MATRIX SELECTION
- WRITE AND READ CONTROLS INCLUDED
- LOW POWER DISSIPATION–150μW/bit at 1 MHz
- LOW CLOCK CAPACITANCE–80pF for 512, 160pF for 1024 Bits
- +5, -5V POWER SUPPLIES
- STANDARD PACKAGE–10 LEAD TO-100
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

FAST ACCESS SWAPPING MEMORY SYSTEMS
LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST BUFFER MEMORIES
CRT REFRESH MEMORIES
DELAY LINE MEMORY REPLACEMENT
DRUM MEMORY REPLACEMENT

PROCESS TECHNOLOGY

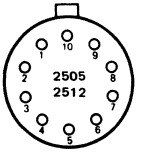
Use of low threshold *silicon gate technology* allows high speed (3MHz typical) while reducing power dissipation and clock input capacitance dramatically as compared to other technologies. The use of low voltage circuitry minimizes power dissipation and facilitates interfacing with bipolar integrated circuits.

BIPOLAR COMPATIBILITY

The signal inputs of these registers can be driven directly by standard bipolar integrated (TTL, DTL, etc.) or by MOS circuits. The bare drain output stage provides driving capability for both MOS and bipolar integrated circuits (one standard TTL load).

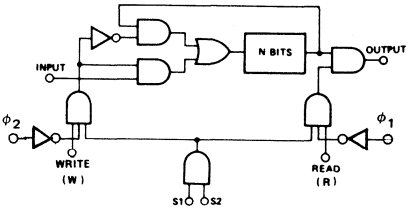
PIN CONFIGURATION (Top View)

K PACKAGE



1. Select 1
2. Write
3. Input
4. ϕ_1 Output Clock
5. V_{CC}
6. ϕ_2 Input Clock
7. Output
8. Read
9. Select 2
10. V_{DD}

BLOCK DIAGRAM



NOTES:
N = 512 or 1024 '0' = 0V, '1' = +5V.
When S1 or S2 is '0' Data Recirculates
When S1 and S2 are '1' see truth table

TRUTH TABLE

WRITE	READ	FUNCTION
0	0	Recirculate, Output is '0'
0	1	Recirculate, Output is Data
1	0	Write Mode, Output is '0'
1	1	Read/Write, Output is Data

PART IDENTIFICATION TABLE

PART NO.	BIT LENGTH	PACKAGE
2505K	512	10 pin TO - 100
2512K	1024	10 pin TO - 100

MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature (2)	0°C to +70°C
Storage Temperature	-65°C to +150°C
Power Dissipation (2)	535mW@T_A>70°C
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+0.3V to -20V

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. All inputs are protected against static charge.
4. See "Minimum Operating Frequency" graph for low limits on data rep. rate.
5. Parameters are valid over operating temperature range unless otherwise specified.
6. All voltage measurements are referenced to ground.
7. Manufacturer reserves the right to make design and process changes and improvements.
8. Typical values are at +25°C and nominal supply voltages.
9. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are $V_{IH} = V_{CC} - 1.85V$ and $V_{IL} = V_{CC} - 4.15V$.
10. V_{OL} is a function of the input characteristics of the driven TTL/DTL gate I_{OI} and V_{CLAMP} and the value of the pull down resistor (R_L).

DC CHARACTERISTICS $T_A = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$; $V_{DD} = -5V \pm 5\%$ unless otherwise noted.

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	$V_{IN} = -5.5V$; $T_A = 25°C$
I_{LO}	Output Leakage Current		10	1000	nA	$V_{\phi 1} = V_{\phi 2} = -12V$, $V_{DD} = -5V$; $V_{OUT} = -5.5V$; $T_A = 25°C$
I_{LC}	Clock Leakage Current		10	1000	nA	$V_{ILC} = 12V$; $T_A = 25°C$
I_{DD}	Power Supply Current 2505		15	25	mA	Continuous Operation; ϕ pW = 150nS, 1MHz
	2512		25	35	mA	$V_{ILC} = -12V$; $T_A = 25°C$ $V_{DD} = -5.5V$
V_{IL}	Input "Low" Voltage	-5.0		+0.6	V	See Note 9
V_{IH}	Input "High" Voltage	+3.4		5.3	V	See Note 9
V_{ILC}	Clock Input "Low" Voltage	-12.0		10.0	V	
V_{IHC}	Clock Input "High" Voltage	4.0		5.3	V	

EXAMPLE TIMING DIAGRAM

4-BIT RECIRCULATING SHIFT REGISTER

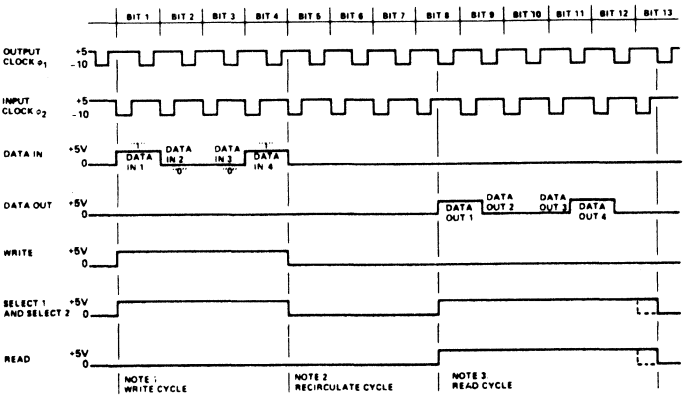


Figure 1

NOTE 1: (WRITE cycle)

The positive and negative going edge of the "W", "S1", "S2" controls are coincident with the negative going edge of the input clock (ϕ_2). The "Read" control may be either "1" or "0".

NOTE 2: (RECIRCULATE cycle)

Data recirculates if one or more of the following control lines are "0", S1, S2 and W. Read may be either "1" or "0".

NOTE 3: (READ cycle)

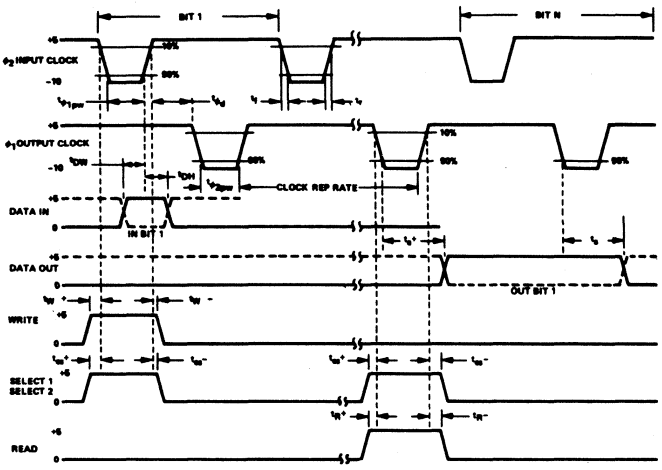
The positive going edge of the "Read", "S1", "S2" controls are coincident with the negative edge of the output clock (ϕ_1). The negative going edge of R, S1, S2 is coincident with the negative going edge of either clock pulse succeeding the last desired data output bit. W may be either "1" or "0".

Figure 1 is a simplified illustration of the timing of a 4-bit recirculating shift register showing the 3 basic modes of operation.

CONDITIONS OF TEST

Input rise and fall times: 10 nsec Output load is 1 TTL gate

TIMING DIAGRAM



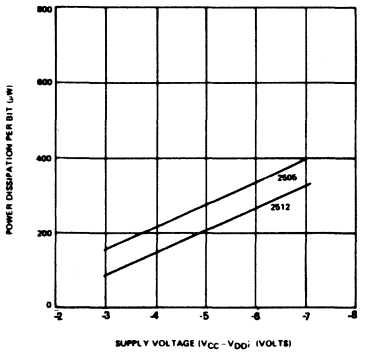
NOTE:
1. N=512 for 2505, N=1024 for 2512
2. Note that the Read Input is AND'ed with $\overline{\phi_1}$; therefore this function is not valid until ϕ_1 occurs.

AC CHARACTERISTICS T_A=+25°C V_{CC}=+5V (9), V_{DD}=−5V ± 5%; V_{ILC}=-11V

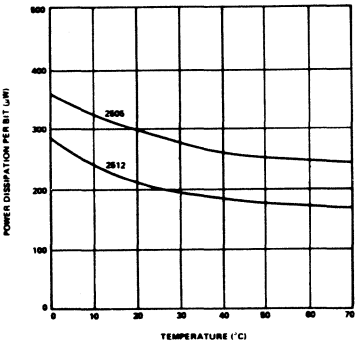
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
Frequency	Clock Data Rep Rate	.0005 (Note 4)	3	2.5	MHz	W = R = V_{CC}
$t_{\phi pw}$	Clock Pulse Width	180			nsec	
$t_{\phi d}$	Clock Pulse Delay	10			nsec	
t_r;t_f	Clock Pulse Transition			1	μsec	
t_{DW}	Data Write (Setup) Time	150			nsec	
t_{DH}	Data to Clock Hold Time	10			nsec	
t_{a+};t_{a-}	Clock to Data Out Delay			100	nsec	
t_{R-};t_{CS-} $t_{W\ -}$	Clock to "Read" or "Chip Select" or "Write" Timing	0			nsec	
t_{R-};t_{CS+} $t_{W\ +}$	Clock to "Read" or "Chip Select" or "Write" Timing	0			nsec	
C_{in}	Input Capacitance			5	pF	1 MHz; V_I=V_{CC}; V_{AC}= 25mV p-p
C_{out}	Output Capacitance			5	pF	1 MHz; V_O=V_{CC}; V_{AC}= 25mV p-p
C_ϕ	Clock Capacitance 2505 2512			50 100	pF pF	1 MHz; V =V_{CC};V_{AC}= 25mV p-p
V_{OL}	Output "Low" Voltage		-1.0		V	R_L = 3.0K; 1 TTL Load (I_L = 1.6mA) Note 10
V_{OH1}	Output "High" Voltage Driving 1 TTL Load	2.4	3.5		V	R_L = 3.0K; 1 TTL Load (I_L = 100μA)
V_{OH2}	Output "High" Voltage Driving MOS	3.6	4.0		V	R_L = 5.6K; C_L = 10 pF

CHARACTERISTICS CURVES

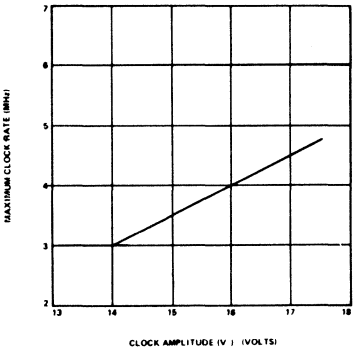
POWER DISSIPATION/BIT VERSUS SUPPLY VOLTAGE



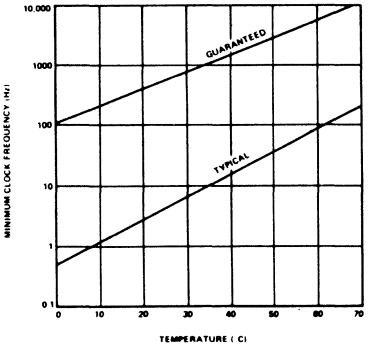
POWER DISSIPATION/BIT VERSUS TEMPERATURE



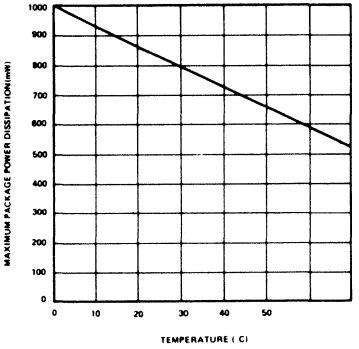
MAXIMUM CLOCK RATE VERSUS CLOCK AMPLITUDE



MINIMUM OPERATING CLOCK FREQUENCY



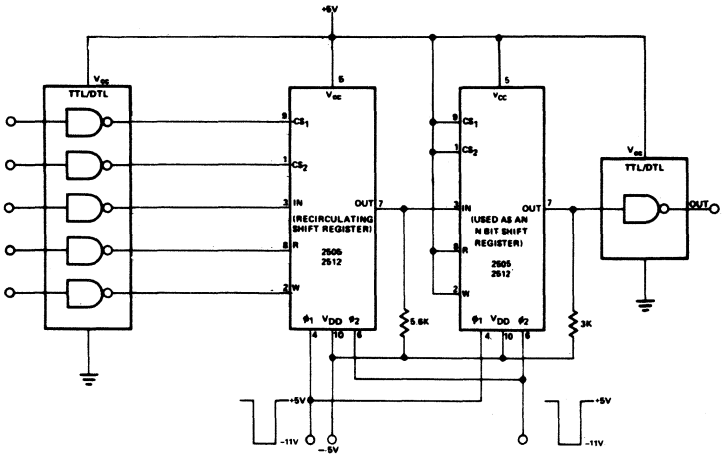
MAXIMUM PACKAGE POWER DISSIPATION VERSUS TEMPERATURE



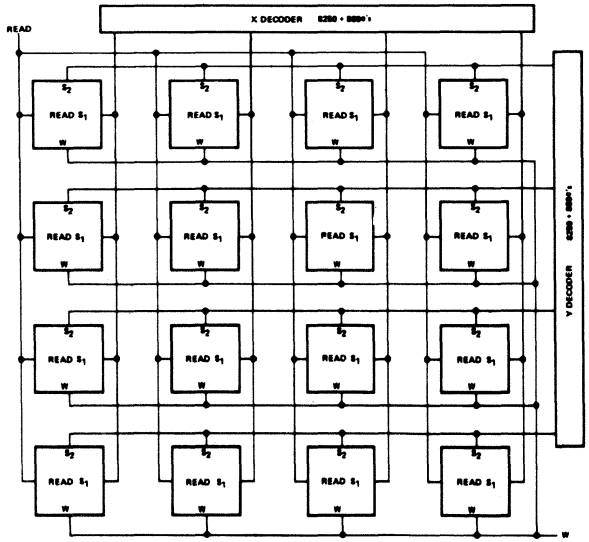
NOTE:
Conditions for Typical Curves = V_{CC}=+5V, V_{DD}=−5V, Clock Duty Cycle=35°C, f_{CLK}=2.5MHz, $V_{\phi p\text{-}p}$=16V, ϕ_{PW} =180ns, T_A=25°C unless otherwise noted

APPLICATIONS DATA

TTL/DTL/MOS INTERFACES

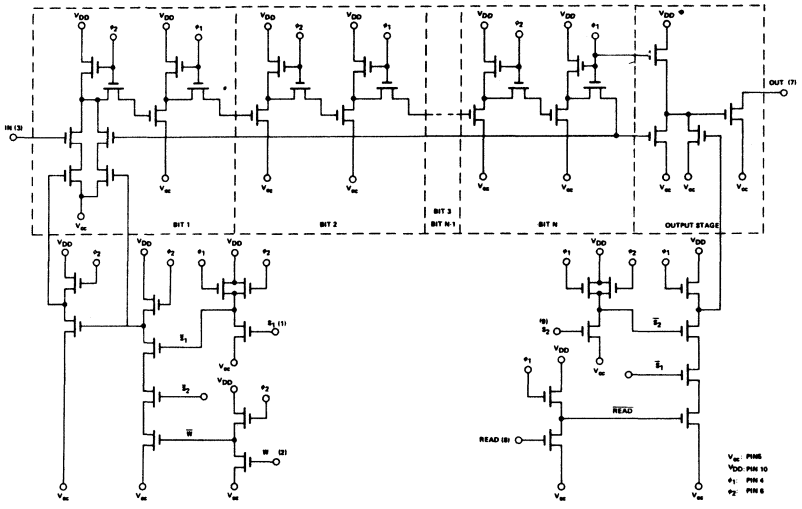


MATRIX CHIP SELECT LOGIC



NOTES:
1. Outputs common for each plane
2. All inputs common for each plane
3. All ϕ_1's common
4. All ϕ_2's common
5. All V_{CC} common
6. All V_{DD} common

CIRCUIT SCHEMATIC



NOTE: N = 512 for 2505
N = 1024 for 2512

signetics

DUAL 100-BIT DYNAMIC SHIFT REGISTER

SILICON GATE MOS 2500 SERIES

2506
2507
2517

DESCRIPTION

These Signetics 2500 Series dual 100-Bit dynamic shift registers consist of enhancement mode P-channel MOS devices integrated on a single monolithic chip. They use two clock phases.

FEATURES

- HIGH FREQUENCY OPERATION
  4 MHz TYPICAL CLOCK RATE
- TTL, DTL COMPATIBLE
- LOW POWER DISSIPATION — 400 μW/BIT AT 1 MHz
- LOW CLOCK CAPACITANCE 40pF MAXIMUM
- LOW OUTPUT IMPEDANCE — 300 OHMS TYPICAL
- BARE DRAIN AND MOS RESISTOR VERSIONS AVAILABLE
- STANDARD PACKAGES — 8 LEAD TO-5 AND 8 LEAD SILICONE DIP
- SIGNETICS P-MOS SILICON GATE AND SILICONE PACKAGING TECHNOLOGIES

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST BUFFER MEMORIES

PROCESS TECHNOLOGY

Use of the low threshold silicon gate technology allows high speed (3 MHz guaranteed), while reducing power dissipation by a factor of 2 and reducing clock input capacitance dramatically as compared to conventional MOS technologies.

SILICONE PACKAGING

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric material over the silicon gate-oxide-substrate structure provides an ion barrier. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability, demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers. For further information reference Signetics - "Silicone Package Qualification Report".

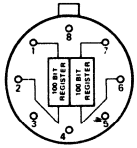
BIPOLAR COMPATIBILITY

The dual 100 bit device can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.) or by MOS circuits. The design of the output stage provides driving capability for MOS or bipolar IC's.

It is available in bare drain configuration or with internal pull down resistor values of 7.5k or 20k to provide easier interfacing with other MOS circuitry.

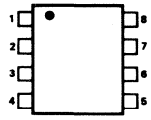
PIN CONFIGURATIONS (TOP VIEW)

T PACKAGE



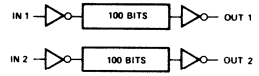
1. Input 1
2. Output 1
3. Input Clock (ϕ_2)
4. V_{CC}
5. Output Clock (ϕ_1)
6. Output 2
7. Input 2
8. V_{DD}

V PACKAGE



1. Output Clock (ϕ_1)
2. Output 2
3. Input 2
4. V_{DD}
5. Input 1
6. Output 1
7. Input Clock (ϕ_2)
8. V_{CC}

BLOCK DIAGRAM



PART IDENTIFICATION TABLE

PART NO.	OUTPUT	PACKAGE
2506 T	Bare Drain	8 Pin TO-5
2506 V	Bare Drain	8 Pin DIP
2507 T	7.5k Pull Down	8 Pin TO-5
2507 V	7.5k Pull Down	8 Pin DIP
2517 T	20k Pull Down	8 Pin TO-5
2517 V	20k Pull Down	8 Pin DIP

MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient	0°C + 70°C
Storage Temperature	-65°C + 150°C
Power Dissipation (Note 2) @ T_A=70°C	
T Package	535mW
V Package	455mW
Clock Input Voltages with respect to V_{CC}(3)	+0.3 to -20V
Supply and Data Input Voltages with respect to V_{CC}(3)	+0.3 to -12V

NOTES:
1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W (T package) or 175° C/W (V package).
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}. V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.
9. V_{OL} (for this bare drain device) is a function only of the driven gate characteristics together with the external pull-down resistor. (R_{PD}).
10. See Figure 2 for definitions.
11. Logic Convention: Data Lines - Positive; Clocks - Negative.

DC CHARACTERISTICS

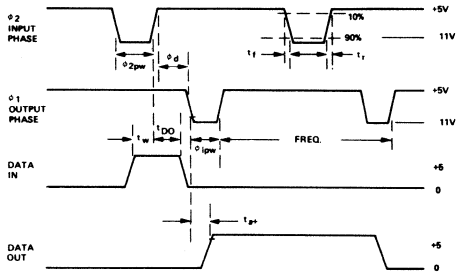
T_A = 0°C to +70°C; V_{DD} = -5V ±5%; V_{CC} = +5 (8); unless otherwise noted(Notes: 4,5,6,7).

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	Input Load Current (Input 1)		10	500	nA	+5V ON OUT 1, ϕ1, ϕ2, V_{CC}, IN 2, OUT 2, IN 1 = −5.5V, V_{DD} = −4.5V, T_A = 25°C
I_{LI}	Input Load Current (Input 2)		10	500	nA	+5V ON OUT 2, ϕ1, ϕ2, V_{CC}, IN 1, OUT 1, IN 2 = −5.5V, V_{DD} = −4.5V, T_A = 25°C
I_{LO}	Output Leakage Current (OUT 1) (Notes 9 & 10)		10	1000	nA	+5V ON IN 1, V_{CC}, OUT 2, ϕ2, IN 2, V_{DD}, OUT 1 = −5.5V ϕ1 = −10V, T_A = 25°C (2506 Only)
I_{LO}	Output Leakage Current (OUT 2) (Notes 9 & 10)		10	1000	nA	+5V ON IN 1, OUT 1, V_{CC}, ϕ2, IN 2, V_{DD}, OUT 2 = −5.5V, ϕ = −10V, T_A = 25°C (2506 Only)
I_{LC}	Clock Leakage Current (ϕ1)		10	1000	nA	Vϕ1 = −12 V, V_{DD} = −4.5V All other pins +5V, T_A = 25°C
I_{LC}	Clock Leakage Current (ϕ2)		10	1000	nA	Vϕ2 = −12V, V_{DD} = −4.5V All other pins +5V T_A = 25°C
V_{IL}	Input "Low" Voltage (Note 11)	−5		1.05	V	
V_{IH}	Input "High" Voltage (Note 11)	3.2		5.3	V	
C_{IN}	Input Capacitance (Inputs 1 & 2)		2.5	5	pF	V_{IN} = V_{CC}, 1 MHz, 25 mV p-p
C_ϕ	Clock Input Capacitance (ϕ1, ϕ2)		25	40	pF	V_ϕ = V_{CC} , 1 MHz, 2 5 mV p-p
V_{IHC}	Clock Input "High" Voltage	4		5.3	V	
V_{ILC}	Clock Input "Low" Voltage	−12		−10	V	

CONDITIONS OF TEST

Data amplitude +1.05 to +3 2 Input rise and fall times: 10 nsec. Output load is 1 TTL gate.

TIMING DIAGRAM



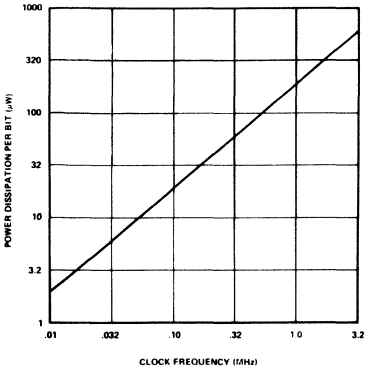
AC CHARACTERISTICS

$T_A = 25°C$; $V_{DD} = -5V \pm 5\%$; $V_{CC} = +5V$ (8) ; $V_{ILC} = -11V$

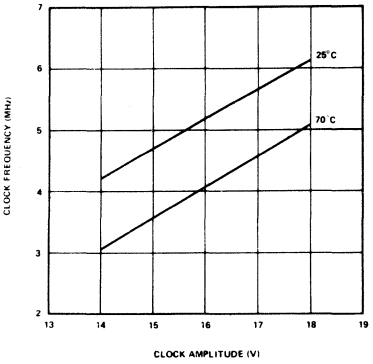
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
Frequency	Clock Rep Rate	0006	4	3	MHz	
ϕ IPW	Clock Pulse Width ϕ 1	150			nsec	@ 3MHz.
ϕ 2PW	Clock Pulse Width ϕ 2	100			nsec	@ 3MHz.
ϕ_d	Clock Pulse Delay	10			nsec	@ 3MHz
t_r, t_f	Clock Pulse Transition	10		1000	nsec	
t_W	Data Write Time (Set-Up)	75				
t_{DO}	Data In Overlap	10				$t_{r\phi 2} = t_{r\phi 1} = 10nS$
t_{a+}	Clock to Data Out		90	150		$V\phi = V_{CC} - 16V$, DATA OUT =+2.5V
V_{OH1}	Output "High" Voltage driving MOS (Note 11)	3.4	4.0		V	$R_{INT} = 7.5k$ nom., $C_L = 10pF$, 2507 Only, $R_{INT} = 20k$ nom. 2517 only
V_{OH2}	Output "High" Voltage driving TTL (Note 11)	3.0	3.5		V	$R_L = 3.3k$, $V_{DD} = -5V$ 2506 only
I_{DD}	Power Supply Current (V_{DD})		12	26	mA	Outputs @ logic "0" or "1", 3MHz, $\phi_1 = 150ns$, $\phi_2 = 100ns$

CHARACTERISTIC CURVES

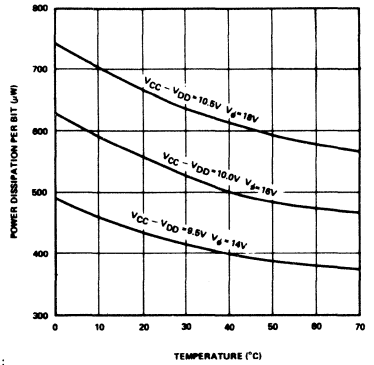
POWER DISSIPATION PER BIT VERSUS FREQUENCY



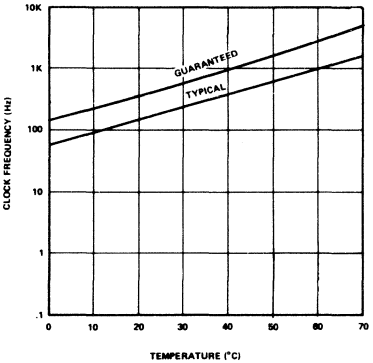
TYPICAL CLOCK FREQUENCY VERSUS CLOCK AMPLITUDE



POWER DISSIPATION BIT VERSUS TEMPERATURE



MINIMUM OPERATING CLOCK RATE

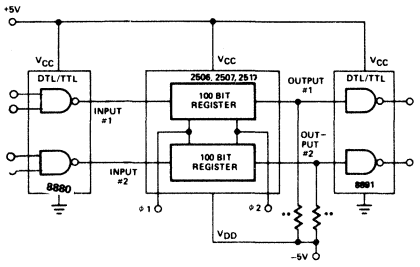


NOTE:
Contitions for Typical Curves: V_{CC}=+5V, V_{DD}=-5V. V_{ILC}=-11V, ϕ_{PW1}=150ns, ϕ_{PW2}=100ns, f=3MHz, T_A=+25°C unless otherwise noted.

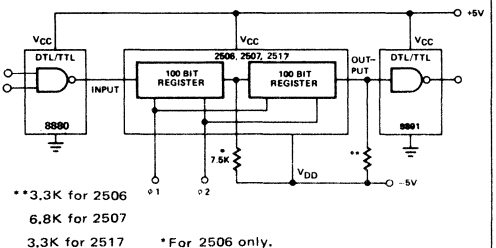
APPLICATIONS DATA

DTL/TTL/MOS INTERFACES

100-BIT DELAY



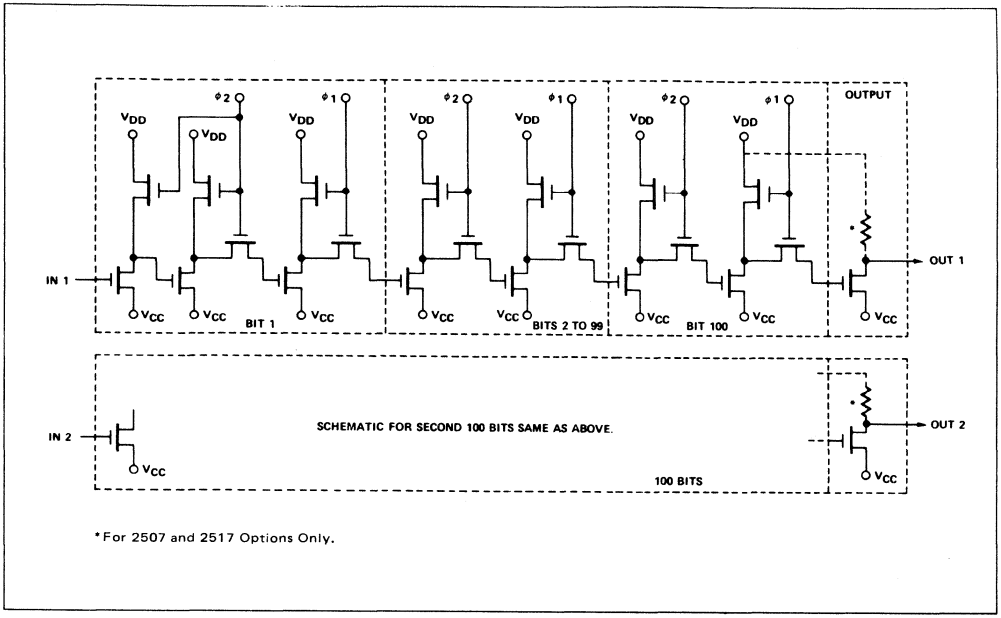
200-BIT DELAY



**3.3K for 2506
6.8K for 2507
3.3K for 2517

*For 2506 only.

CIRCUIT SCHEMATIC



*For 2507 and 2517 Options Only.

signetics

TRI-STATE OUTPUT DUAL 50-100-200 BIT STATIC SHIFT REGISTERS

SILICON GATE MOS 2500 SERIES

2509
2510
2511

DESCRIPTION

These Signetics 2500 Series Dual 50, 100, and 200 bit recirculating static shift registers consist of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip. Internal recirculation logic plus TTL/DTL level clock signals plus TRI-STATE outputs are provided for maximum interfacing ease.

FEATURES

- TRI-STATE MOS OUTPUTS - PROVIDE POWERFUL BUSSING CAPABILITY
- TTL/DTL COMPATIBLE CLOCKS - PROVIDE EXTREMELY LOW CLOCK CAPACITANCE
- RECIRCULATION PATH ON CHIP
- THREE BIT LENGTHS AVAILABLE
- HIGH FREQUENCY OPERATION
- 1.5MHz GUARANTEED CLOCK RATE
- TTL, DTL COMPATIBLE SIGNALS
- STANDARD PACKAGES - 10 LEAD TO-100, 14 PIN DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST STATIC BUFFER MEMORIES
CRT REFRESH MEMORIES - LINE STORAGE

SPECIAL FEATURES

The three clock phases used by the register cells are generated internally by an on-chip generator. This clock generator is controlled by a single TTL/DTL 5V logic level input.

The output has three states:
"1" low impedance to +5V
"0" low impedance to -5V
"OFF" high impedance ≃ 10 M ohm
The "OFF" state is controlled by the Output Enable control input.

PROCESS TECHNOLOGY

Use of low threshold silicon gate technology allows high speed (1.5MHz Guaranteed) while reducing power dissipation and clock input capacitance dramatically as compared to conventional technologies.

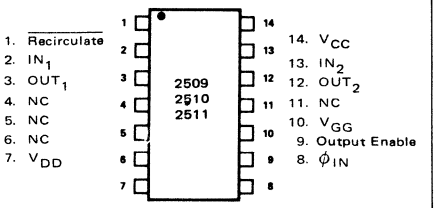
The use of low voltage circuitry minimizes power dissipation and facilitates interfacing with bipolar integrated circuits.

BIPOLAR COMPATIBILITY

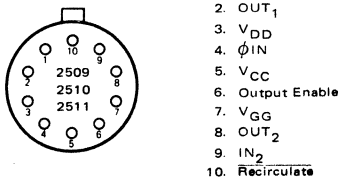
The clock and signal inputs of these registers can be driven directly by standard bipolar integrated (TTL, DTL, etc.) circuits, by CMOS circuits, or by other MOS circuits. The TRI-STATE output stage provides sufficient current to drive one standard TTL load.

PIN CONFIGURATIONS (Top View)

A PACKAGE



K PACKAGE



PART IDENTIFICATION TABLE

PART NUMBER	BIT LENGTH	PACKAGE
2509K	Dual 50	10 Pin, TO-100
2509A	Dual 50	14 Pin, DIP
2510K	Dual 100	10 Pin, TO-100
2510A	Dual 100	14 Pin, DIP
2511K	Dual 200	10 Pin, TO-100
2511A	Dual 200	14 Pin, DIP

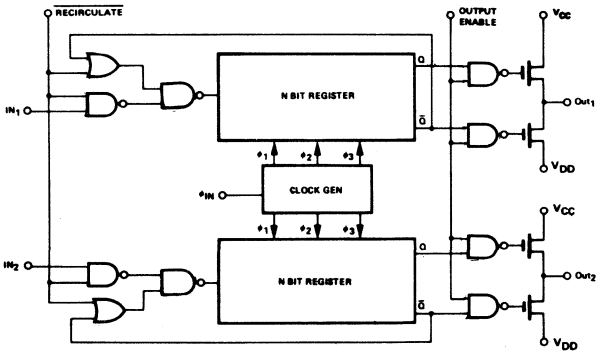
MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature (2)	0°C to +70°C
Storage Temperature	-65°C to +150°C
Package Power Dissipation (A & K) (Note 2) @ T_A = 70°C	535mW
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC} (3)	+0.3V to -20V

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W.
3. All inputs are protected against static charge accumulation.
4. Parameters are valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nomimal supply voltages.
8. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are $V_{IH} = V_{CC} - 1.85V$ and $V_{IL} = V_{CC} - 4.15V$.

BLOCK DIAGRAM



NOTES:
1: If output enable = "0", output is "off".
2: If output enable = "1", see Truth Table.

TRUTH TABLE:

$\overline{\text{RECIRCULATE}}$	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is Written
1	1	"1" is Written

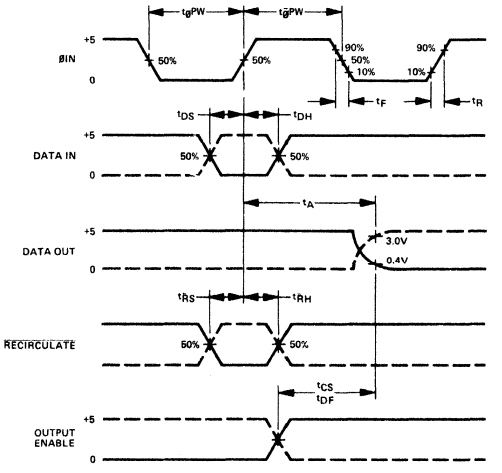
NOTE: "0" = OV; "1" = +5V.

DC CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = +5V (8); V_{DD} = -5V ±5%; V_{GG} = -12V ±5% unless otherwise noted. (Notes 4,5,6,7)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} =-5.5V, T_A = 25°C
I_{LO}	Output Leakage Current		10	1000	nA	V_{CE} =1.05V,T_A = 25°C, V_{OUT} = -5V
I_{LC}	Clock Leakage Current		10	500	nA	V_{ILC} = GND, T_A = 25°C
I_{DD}	Power Supply Current					
	(Dual 50)		6.5	15	mA	Continuous Operation
	(Dual 100)		12	30	mA	F = 1.5MHz, T_A = 25°C
	(Dual 200)		20	40	mA	
I_{GG}	Power Supply Current		4.5	7.5	mA	
V_{IL}	Input "Low" Voltage			+0.6	V	Note 8
V_{IH}	Input "High" Voltage	+3.4		5.3	V	Note 8
V_{ILC}	Clock Input "Low" Voltage	-5		+0.6	V	Note 8
V_{IHC}	Clock Input "High" Voltage	+3.4		5.3	V	Note 8

TIMING DIAGRAM



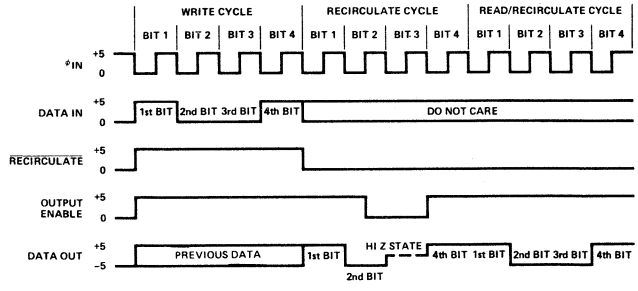
t_R = t_F <10 NSEC FOR ALL INPUTS

AC CHARACTERISTICS

V_{CC} = +5V (8); V_{DD} = -5V ±5%; V_{ILC} = +0.4V to 4V; V_{GG} = -12V ±5%; T_A = 0° C to +70°C

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
Frequency	Clock Rep Rate	DC	3	1.5	MHz	
$t_{\phi}PW$	Clock Pulse Width	.290	.150	100	μsec	
$t_{\overline{\phi}}PW$	$\overline{\text{Clock}}$ Pulse Width	.210		DC	μsec	
t_R, t_F	Clock Pulse Transition			1	μsec	
t_{DS}	Data Write (Set-up) Time	50			nsec	
t_{DH}	Data to Clock Hold Time	50			nsec	
t_A	Clock to Data Out Delay		200	350	nsec	
t_A	Clock to Data Out Delay			500	nsec	I_{OL} = 1.6mA
t_{CS}	Output Enable to Data Out			300	nsec	
t_{DE}	Output Enable to Data Out Disconnect			300	nsec	
C_{IN}	Input Capacitance			5	pF	@ 1 MHz; $V_{IN} = V_{CC}$; V_{AC} = 25mV p-p
C_{OUT}	Output Capacitance			5	pF	@ 1 MHz; $V_{OUT} = V_{CC}$; V_{AC} = 25mV p-p
C_{ϕ}	Clock Capacitance			5	pF	@ 1 MHz; $V_{\phi} = V_{CC}$; V_{AC} = 25mV p-p
V_{OL}	Output "Low" Voltage			+0.5	V	I_{OL} = 1.6mA
V_{OHI}	Output "High" Voltage	+3.8	3.5		V	I_{OH} = 100μA
	Driving MOS	3.6				

TIMING EXAMPLE FOR 4-BIT SHIFT REGISTER



WRITE CYCLE

THE POSITIVE-GOING EDGE OF THE RECIRCULATE CONTROL IS COINCIDENT WITH THE NEGATIVE-GOING CLOCK EDGE. THE OUTPUT ENABLE CONTROL MAY BE EITHER "1" OR "0". IF IT IS "1", PREVIOUS DATA WILL BE READ, AND THE 1st BIT WILL BE READ AFTER THE FOURTH RISING CLOCK EDGE.

RECIRCULATE CYCLE

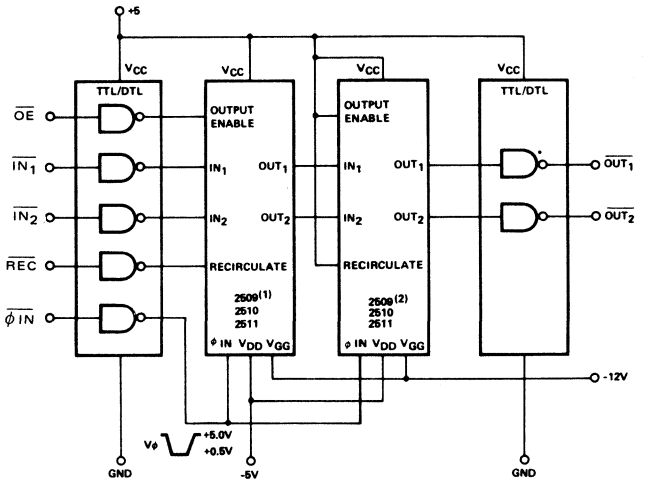
DATA RECIRCULATES WHILE THE RECIRCULATE CONTROL IS "0". OUTPUT ENABLE MAY BE EITHER "1" OR "0". IF IT IS "0", THE OUTPUT IS IN THE HIGH IMPEDANCE STATE'

READ/RECIRCULATE CYCLE

DATA IS READ OUT WHILE THE OUTPUT ENABLE IS "1". DATA IS ALSO RECIRCULATED AS LONG AS THE RECIRCULATE CONTROL is "0".

APPLICATIONS INFORMATION

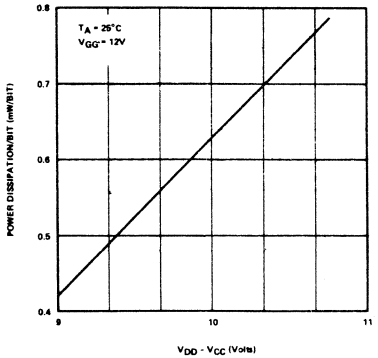
TTL/DTL/MOS INTERFACES



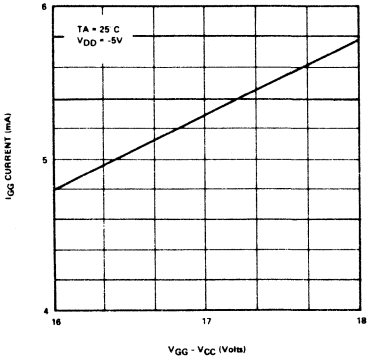
NOTES:
1. Register used as a recirculating register.
2. Register used as serial in/serial out shift register.

TYPICAL CHARACTERISTIC CURVES

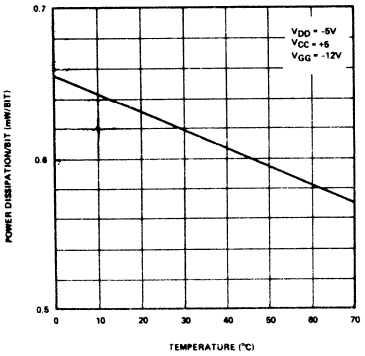
POWER DISSIPATION/BIT VERSUS V_{DD} SUPPLY VOLTAGE



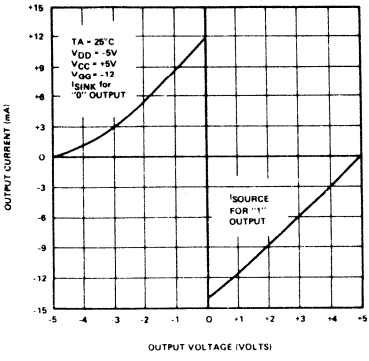
I_{GG} CURRENT VERSUS V_{GG} SUPPLY VOLTAGE



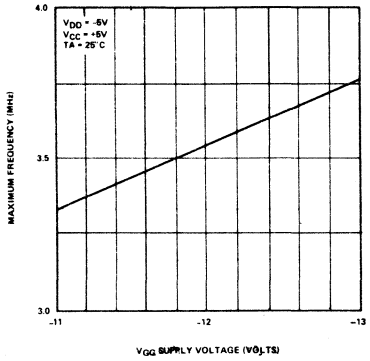
POWER DISSIPATION/BIT VERSUS TEMPERATURE



OUTPUT VOLTAGE VERSUS OUTPUT CURRENT

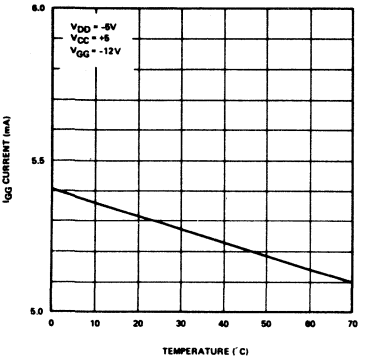


MAXIMUM FREQUENCY VERSUS V_{GG} SUPPLY VOLTAGE

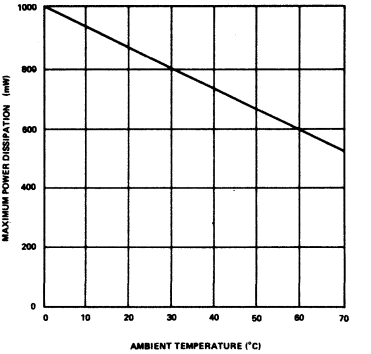


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

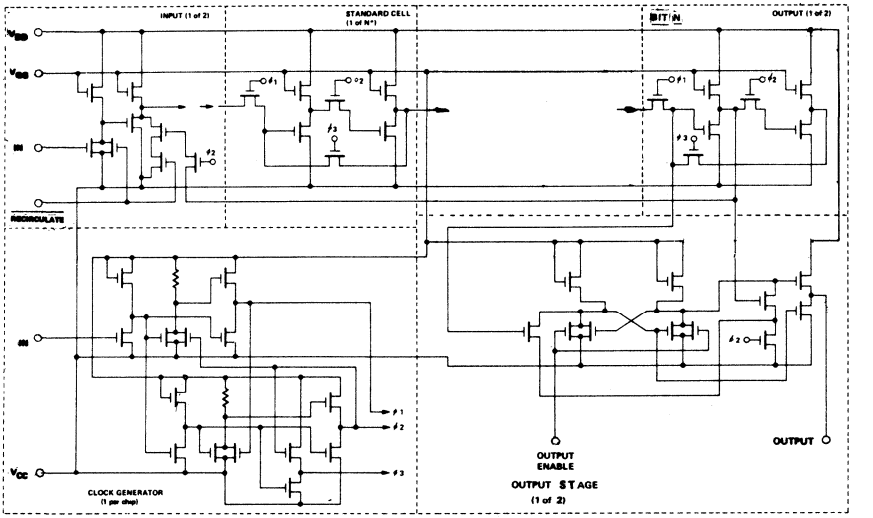
I_{GG} CURRENT VERSUS TEMPERATURE



PACKAGE MAXIMUM POWER DISSIPATION



SCHEMATIC DIAGRAM



signetics

HEX 32-BIT AND 40-BIT STATIC SHIFT REGISTERS

2518
2519

SILICON GATE MOS 2500 SERIES

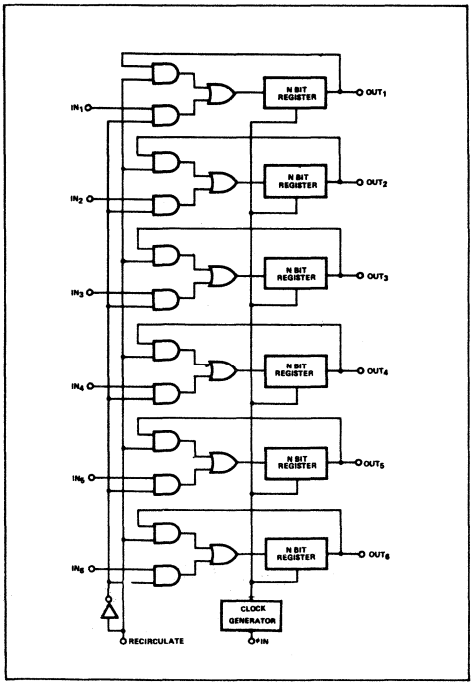
DESCRIPTION

These Signetics 2500 Series hex 32-bit and hex 40-bit recirculating static shift registers consist of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip. Internal recirculation logic plus TTL/DTL level clock signals are provided for maximum interfacing ease.

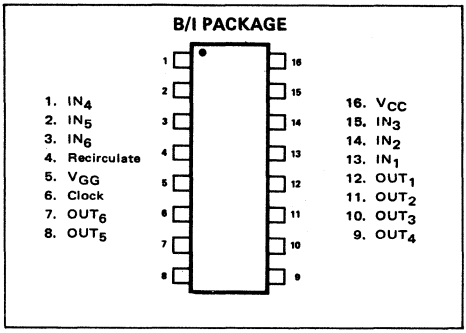
FEATURES

- TYPICAL CLOCK AND DATA RATE = 3MHz
- SINGLE TTL/DTL COMPATIBLE CLOCK
- LOW CLOCK CAPACITANCE
- RECIRCULATION PATH ON CHIP
- TWO BIT LENGTHS AVAILABLE
- SINGLE-ENDED (BARE DRAIN) BUFFERS
- TTL, DTL COMPATIBLE SIGNALS
- STANDARD PACKAGE – 16 PIN DIP
- P-MOS SILICON GATE TECHNOLOGY

BLOCK DIAGRAM



PIN CONFIGURATIONS (Top View)



APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST STATIC BUFFER MEMORIES
CRT REFRESH MEMORIES – LINE STORAGE
LINE PRINTERS
CARD EQUIPMENT BUFFERS

TRUTH TABLE

RECIRCULATE	INPUT	FUNCTION
1	0	Recirculate
1	1	Recirculate
0	0	"0" is Written
0	1	"1" is Written

PART IDENTIFICATION TABLE

PART NUMBER	BIT LENGTH	PACKAGE
2518B	HEX 32	16-Pin Silicone DIP
2518I	HEX 32	16-Pin Ceramic DIP
2519B	HEX 40	16-Pin Silicone DIP
2519I	HEX 40	16-Pin Ceramic DIP

MAXIMUM GUARANTEED RATINGS (1)

Operating Temperature (2)	0°C to +70°C
Storage Temperature	-65°C to +150°C
Package Power Dissipation at T_A = 70°C	640 mW
Data and Clock Input Voltages and Supply Voltages with Respect to V_{CC}	+0.3V to -20V

NOTES

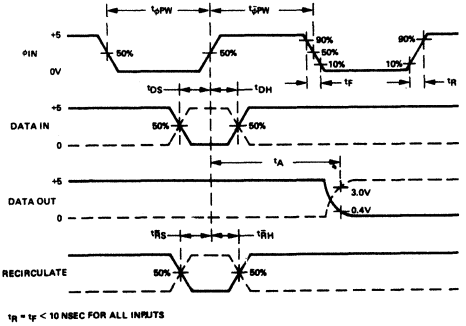
1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 125°C C/W,junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are $V_{IH} = V_{CC} - 1.85V$ and $V_{IL} = V_{CC} - 4.15V$.
9. V_{OL} is dependent on R_L and input characteristics of driven gate.

DC CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = +5V +5V ±5%; V_{GG} = −12V ±5% unless otherwise noted. (Notes: 3,4,5,6,7)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	INPUT LOAD CURRENT		10	500	nA	V_{in} =5.5V, T_A = 25°C
I_{LO}	OUTPUT LEAKAGE CURRENT		10	1000	nA	T_A = 25°C
I_{LC}	CLOCK LEAKAGE CURRENT		10	500	nA	V_{ILC} = GND, T_A = 25°C
I_{GG}	POWER SUPPLY CURRENT		16	25	mA	CONTINUOUS OPERATION T_A = 25°C F = 1.5 MHz
V_{IL}	INPUT "LOW" VOLTAGE			+0.6	V	Note 8
V_{IH}	INPUT "HIGH"VOLTAGE	+3.4		5.3	V	Note 8
V_{ILC}	CLOCK INPUT "LOW" VOLTAGE			+0.6	V	Note 8
V_{IHC}	CLOCK INPUT "HIGH" VOLTAGE	+3.4		5.3	V	Note 8

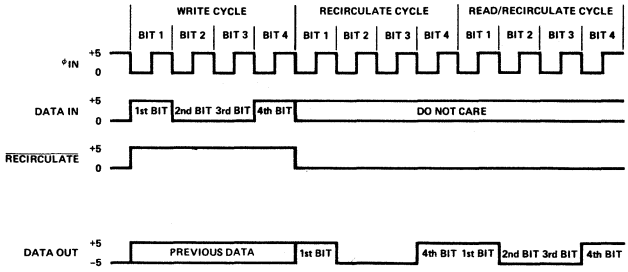
TIMING DIAGRAM



NOTES: A. Input rise and fall times: 10nsec. Output load is 1 TTL gate.

B. For static operation, clock must be stopped in TTL "1" state in order to retain data (see clock pulse width specification).

TIMING DIAGRAM



WRITE CYCLE

THE POSITIVE-GOING EDGE OF THE RECIRCULATE CONTROL IS COINCIDENT WITH THE NEGATIVE-GOING CLOCK EDGE. THE OUTPUT ENABLE CONTROL MAY BE EITHER "1" OR "0". IF IT IS "1", PREVIOUS DATA WILL BE READ, AND THE 1st BIT WILL BE READ AFTER THE FOURTH RISING CLOCK EDGE.

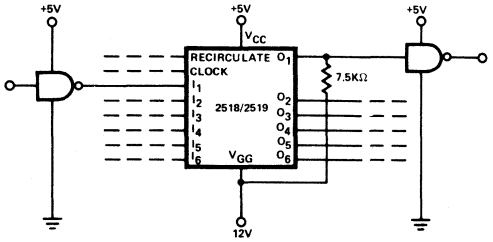
RECIRCULATE CYCLE

DATA RECIRCULATES WHILE THE RECIRCULATE CONTROL IS "0". NEW INPUT DATA IS IGNORED. OUTPUT DATA IS READ OUT DURING THIS TIME.

AC CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V$ $+5V \pm 5\%$; $V_{GG} = -12V \pm 5\%$, $V_{ILC} = 0.4V$ to $4.0V$

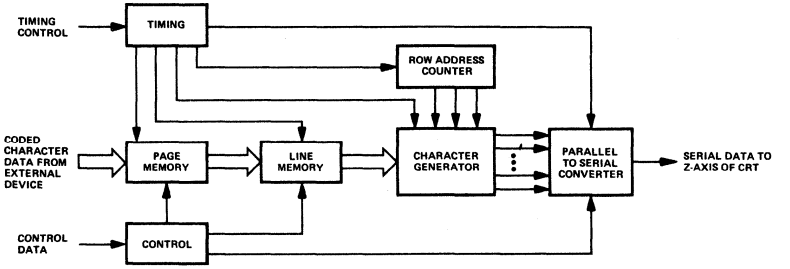
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
FREQUENCY	CLOCK REP RATE	DC	3	2	MHz	See Max Frequency Curve
$t_{\phi PW}$	CLOCK PULSE WIDTH	.300		100	μsec	See Note B
$t_{\overline{\phi}PW}$	CLOCK PULSE WIDTH	.200		DC	μsec	
t_R, t_F	CLOCK PULSE TRANSITION			5	μsec	
t_{DS}	DATA WRITE (SET-UP) TIME	100			nsec	
t_{DH}	DATA TO CLOCK HOLD TIME	50			nsec	
t_A	CLOCK TO DATA OUT DELAY		300	350	nsec	
t_{RS}	RECIRCULATE SET-UP TIME	150			ns	
t_{RH}	RECIRCULATE HOLD TIME	50			ns	
C_{in}	INPUT CAPACITANCE		5	7	pF	@ 1MHz; $V_{in} = V_{CC}$; $V_{AC} = 25mV$ p-p
$C\phi$	CLOCK CAPACITANCE		6	7	pF	@ 1MHz; $V_\phi = V_{CC}$; $V_{AC} = 25mV$ p-p
V_{OL}	OUTPUT "LOW" VOLTAGE		+0.5		V	$I_{OL} = 1.6mA$
V_{OH}	OUTPUT "HIGH" VOLTAGE	+3.8			V	$I_{OH} = 100\mu A$

APPLICATIONS DATA



TTL INTERFACE

APPLICATIONS (Cont'd)

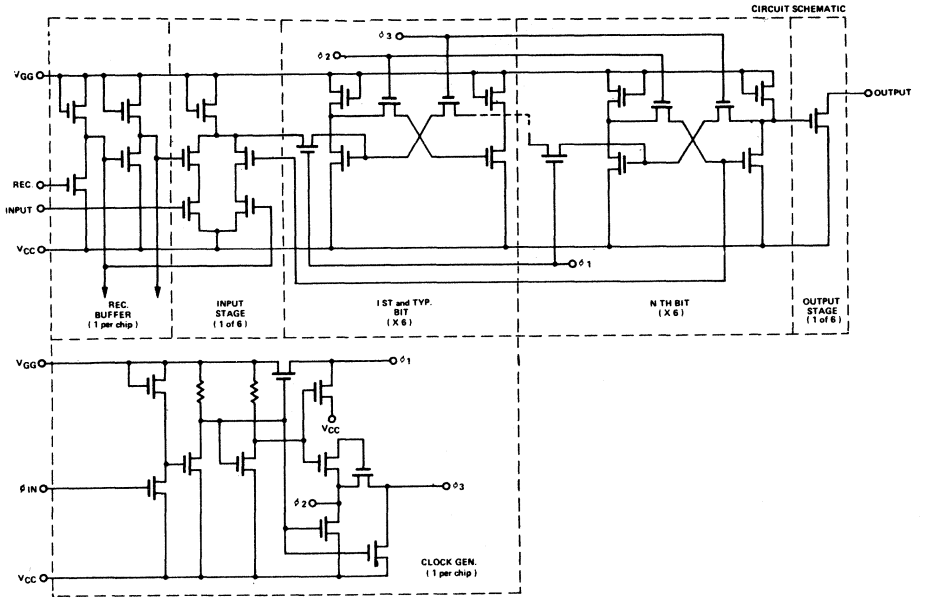


PAGE MEMORY: THIS MEMORY CONTAINS CHARACTER CODES. TYPICALLY, IT CONTAINS THE SAME NUMBER OF CHARACTER CODES AS THE NUMBER OF CHARACTER ON A FULL SCREEN.

LINE MEMORY: THIS MEMORY CONTAINS THE CHARACTER CODES FOR ONE LINE OF THE CRT DISPLAY. THE 2518 AND 2519 WORK WELL AS LINE MEMORIES.

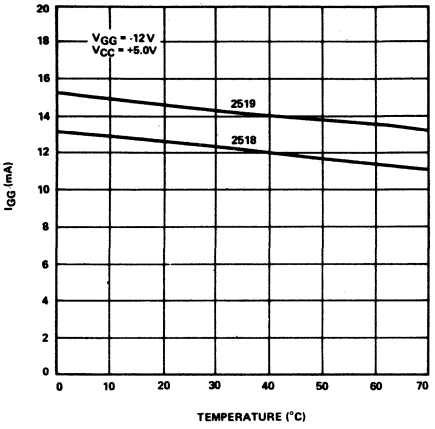
CHARACTER GENERATOR: THE CHARACTER GENERATOR IS TYPICALLY A ROM WHICH CONVERTS CHARACTER CODE INPUTS TO DOT MATRIX BITS AT THE OUTPUT.

CIRCUIT SCHEMATIC

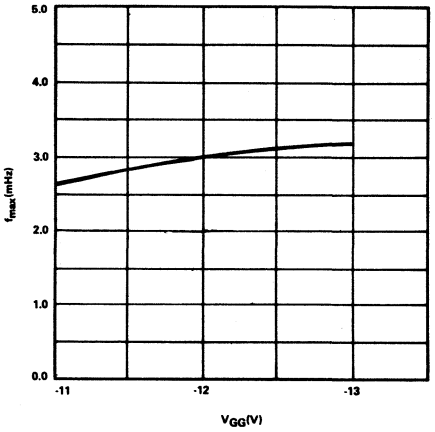


TYPICAL CHARACTERISTIC CURVES

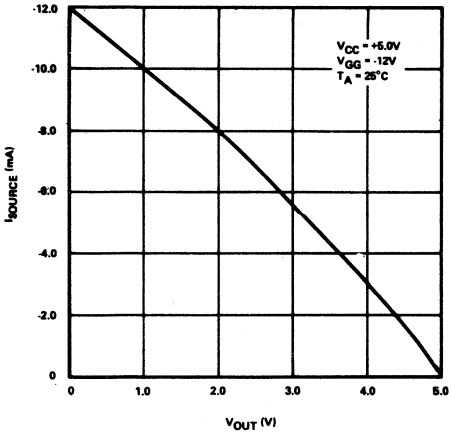
I_{GG} VERSUS TEMPERATURE



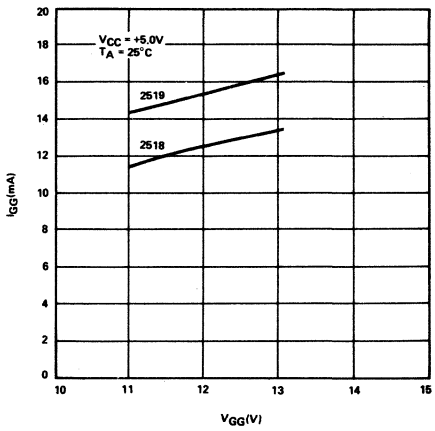
MAXIMUM SHIFT FREQUENCY VERSUS V_{GG}



I_{SOURCE} VERSUS V_{OUT}



I_{GG} VERSUS V_{GG}



signetics

DUAL 128 BIT/DUAL 132 BIT STATIC SHIFT REGISTERS

2521
2522

SILICON GATE MOS 2500 SERIES

DESCRIPTION

These Signetics 2500 Series Dual 128 and 132 bit recirculating static shift registers consist of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip.

FEATURES

- PUSH-PULL OUTPUTS
- TTL/DTL COMPATIBLE CLOCK
- LOW CLOCK CAPACITANCE
- RECIRCULATION PATH ON CHIP
- TWO BIT LENGTHS AVAILABLE
- HIGH FREQUENCY OPERATION – 1.5MHz TYPICAL
- TTL, DTL COMPATIBLE SIGNALS
- STANDARD PACKAGE – 8 LEAD SILICONE DIP
- P-MOS SILICON GATE TECHNOLOGY

APPLICATIONS

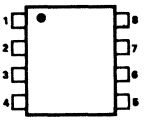
SEQUENTIAL ACCESS MEMORIES
STATIC BUFFER MEMORIES
CRT REFRESH MEMORIES
LINE PRINTERS

BIPOLAR COMPATIBILITY

The clock and signal inputs of these registers can be driven directly by standard bipolar integrated (TTL, DTL, etc.) or by MOS circuits.

PIN CONFIGURATION (Top View)

V PACKAGE



1. $\overline{\text{Recirculate}}$
2. IN_1
3. OUT_1
4. V_{GG}
8. V_{CC}
7. IN_2
6. OUT_2
5. ϕIN

TRUTH TABLE

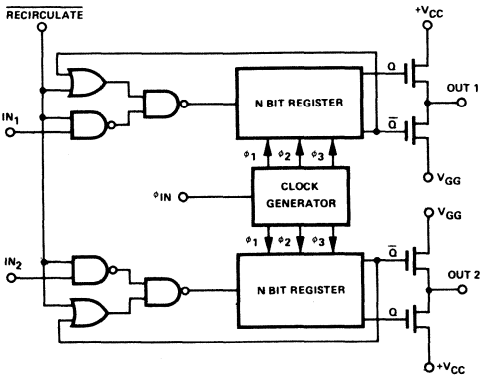
$\overline{\text{RECIRCULATE}}$	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is Written
1	1	"1" is Written

NOTE: "0" = 0V; "1" = +5V.

PART IDENTIFICATION TABLE

PART NUMBER	BIT LENGTH	PACKAGE
2521V	Dual 128	8 Pin DIP
2522V	Dual 132	8 Pin DIP

BLOCK DIAGRAM



MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature (2)	0°C to +70°C
Storage Temperature	-65°C to +150°C
Package Power Dissipation at T_A = 70°C	535 mW
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+0.3V to -20V

NOTES:

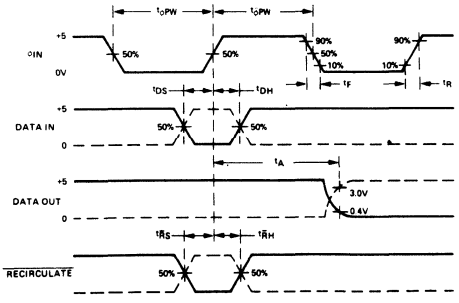
1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserving the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are $V_{IH} = V_{CC} - 1.85V$ and $V_{IL} = V_{CC} - 4.15V$.

DC CHARACTERISTICS T_A = 0°C to +70°C; V_{CC} = +5V +5V ±5%; V_{GG} = −12V ±5% unless otherwise noted.

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	INPUT LOAD CURRENT		10	500	nA	V_{in} = 5.5V, T_A = 25°C
I_{LC}	CLOCK LEAKAGE CURRENT		10	500	nA	V_{ILC} = GND, T_A = 25°C
I_{GG}	POWER SUPPLY CURRENT		28	32	mA	CONTINUOUS OPERATION F = 1.5MHz, T_A=25°C
V_{IL}	INPUT "LOW" VOLTAGE			0.6V	V	See Note 8
V_{IH}	INPUT "HIGH" VOLTAGE	+3.4		5.3	V	
V_{ILC}	CLOCK INPUT "LOW" VOLTAGE			0.6V	V	
V_{IHC}	CLOCK INPUT "HIGH" VOLTAGE	+3.4		5.3	V	

CONDITIONS OF TEST Input rise and fall times: 10 nsec. Output load is 1 TTL gate

TIMING DIAGRAM



NOTES: A $t_R = t_F < 10$ NSEC FOR ALL INPUTS

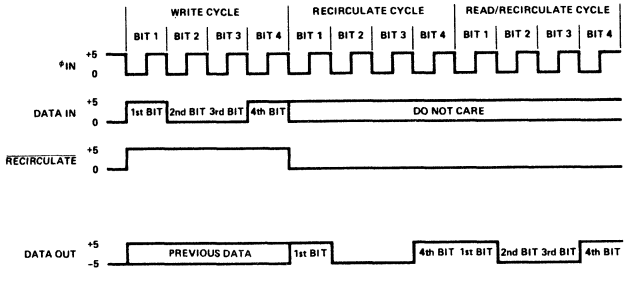
B FOR STATIC OPERATION, CLOCK MUST BE STOPPED IN TTL "1" STATE IN ORDER TO RETAIN DATA (SEE CLOCK PULSE WIDTH SPECIFICATION).

AC CHARACTERISTICS V_{CC} = +5V +5V ±5%; V_{GG} = −12V ±5%; T_A = 0° to +70°C

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
FREQUENCY	CLOCK REP RATE	DC		1.5	MHz	See Maximum Frequency Curve
$t_{\phi PW}$	CLOCK PULSE WIDTH	.350	.100	100	μsec	See Note B
$t_{\overline{\phi} PW}$	CLOCK PULSE WIDTH	.200		DC	μsec	
t_R, t_F	CLOCK PULSE TRANSITION			1	usec	
t_{DS}	DATA WRITE (SET-UP) TIME	75			nsec	
t_{DH}	DATA TO CLOCK HOLD TIME	50			nsec	
t_A	CLOCK TO DATA OUT DELAY		250	350	nsec	
$t_{\overline{RS}}$	$\overline{\text{RECIRCULATE}}$ SET-UP TIME	50			ns	
$t_{\overline{RH}}$	$\overline{\text{RECIRCULATE}}$ HOLD TIME	50			ns	
C_{IN}	INPUT CAPACITANCE			5	pF	@ 1MHz; $V_{in} = V_{CC}$; V_{AC} = 25mV p-p
$C\phi$	CLOCK CAPACITANCE			5	pF	@ 1MHz; $V_\phi = V_{CC}$; V_{AC} = 25mV p-p
V_{OL}	OUTPUT "LOW" VOLTAGE			+0.5	V	I_{OL} = 1.6mA
V_{OH}	OUTPUT "HIGH" VOLTAGE	+3.8			V	I_{OH} = 100μA

EXAMPLE TIMING DIAGRAM FOR 4-BIT SHIFT REGISTER

4 BIT RECIRCULATING SHIFT REGISTER *



WRITE CYCLE

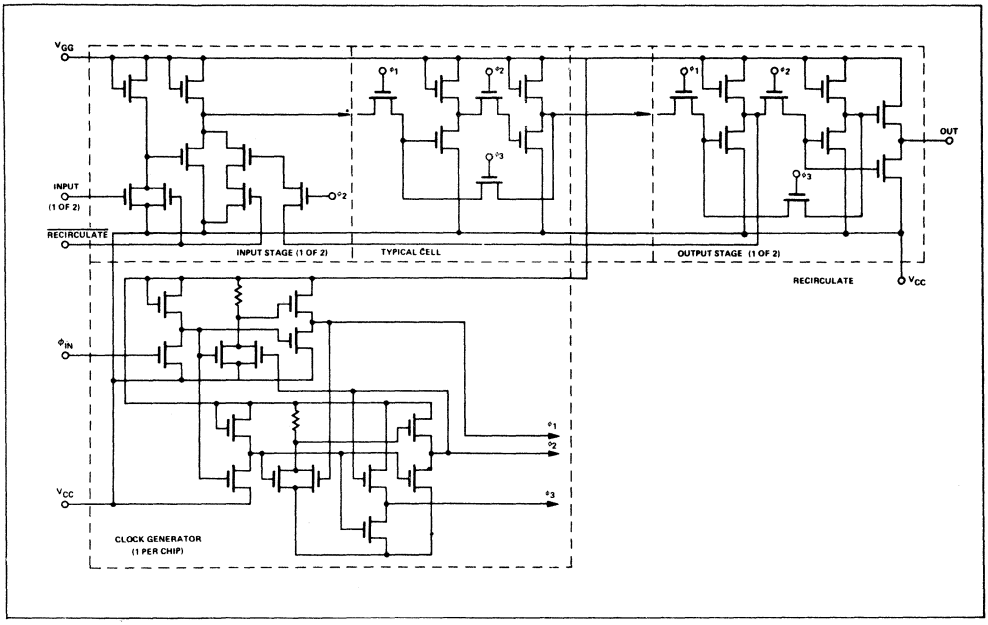
THE POSITIVE-GOING EDGE OF THE RECIRCULATE CONTROL IS COINCIDENT WITH THE NEGATIVE GOING CLOCK EDGE. THE OUTPUT ENABLE CONTROL MAY BE EITHER "1" OR "0". IF IT IS "1", PREVIOUS DATA WILL BE READ, AND THE 1st BIT WILL BE READ AFTER THE FOURTH RISING CLOCK EDGE.

RECIRCULATE CYCLE

DATA RECIRCULATES WHILE THE RECIRCULATE CONTROL IS "0". NEW INPUT DATA IS IGNORED. OUTPUT DATA IS READ OUT DURING THIS TIME.

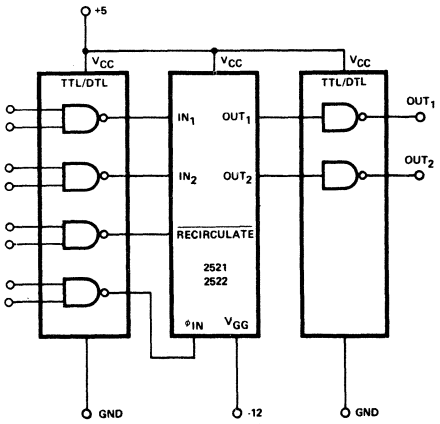
*For clarity, a four bit hypothetical example is shown

SCHEMATIC DIAGRAM



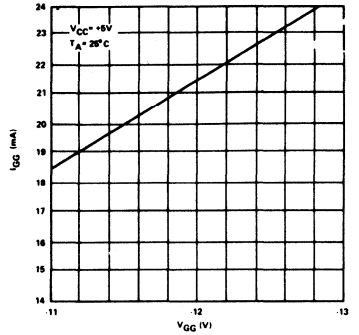
APPLICATIONS DATA

TTL/DTL/MOS INTERFACES

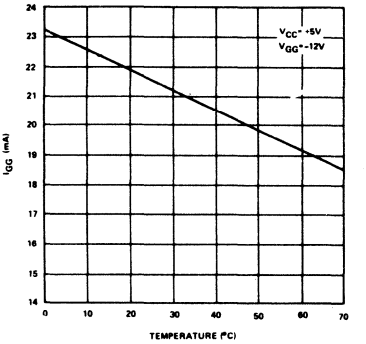


TYPICAL CHARACTERISTIC CURVES

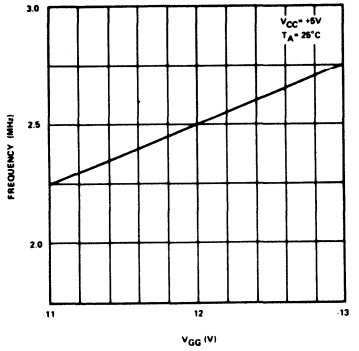
POWER SUPPLY CURRENT VERSUS POWER SUPPLY VOLTAGE



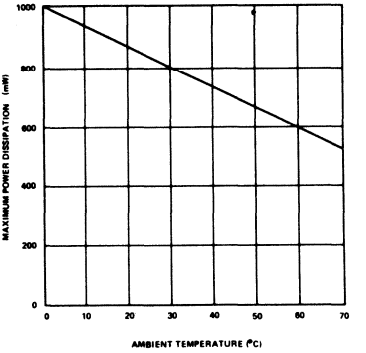
POWER SUPPLY CURRENT VERSUS TEMPERATURE



TYPICAL OPERATING FREQUENCY VERSUS SUPPLY VOLTAGE



PACKAGE MAXIMUM POWER DISSIPATION



signetics

512 AND 1024 BIT RECIRCULATING DYNAMIC SHIFT REGISTERS

2524
2525

SILICON GATE MOS 2500 SERIES

DESCRIPTION

These Signetics 2500 Series 512 and 1024 bit recirculating dynamic shift registers consist of enhancement mode P-channel MOS devices integrated on a single monolithic chip. Internal recirculation logic plus write and read controls are included on the chip.

FEATURES

- **HIGH FREQUENCY OPERATION – 5MHz TYPICAL**
- **SINGLE 512, SINGLE 1024**
- **TTL, DTL COMPATIBLE**
- **WRITE AND READ CONTROLS INCLUDED**
- **LOW POWER DISSIPATION – 200μW/BIT AT 1 MHz**
- **+5, –5 POWER SUPPLIES**
- **STANDARD PACKAGE 8-LEAD DIP**
- **P-MOS SILICON GATE TECHNOLOGY**

APPLICATIONS

FAST ACCESS SWAPPING MEMORY SYSTEMS
LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST BUFFER MEMORIES
CRT REFRESH MEMORIES
DELAY LINE MEMORY REPLACEMENT
DRUM MEMORY REPLACEMENT

PROCESS TECHNOLOGY

Use of low threshold silicon gate technology allows high speed (5MHz typical) while reducing power dissipation and clock input capacitance dramatically as compared to other technologies. The use of low voltage circuitry minimizes power dissipation and facilitates interfacing with bipolar integrated circuits.

BIPOLAR COMPATIBILITY

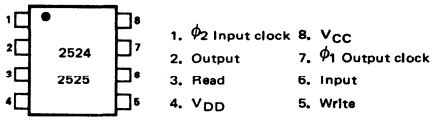
The signal inputs of these registers can be driven directly by standard bipolar integrated (TTL, DTL, etc.) or by MOS circuits. The bare drain output stage provides driving capability for both MOS and bipolar integrated circuits (one standard TTL load).

SILICONE PACKAGING

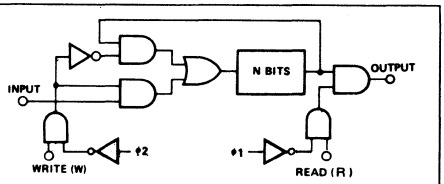
Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric material over the silicon gate-oxide-substrate structure provides an ion barrier. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability and demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers.

PIN CONFIGURATION (Top View)

V PACKAGE



BLOCK DIAGRAM



NOTE
N = 512 or 1024 '0' = 0V, '1' = +5V.

TRUTH TABLE

WRITE	READ	FUNCTION
0	0	Recirculate, Output is '0'
0	1	Recirculate, Output is Data
1	0	Write Mode, Output is '0'
1	1	Read Mode Output is Data

PART IDENTIFICATION TABLE

PART NO.	BIT LENGTH	PACKAGE
2524V	512	8 pin DIP
2525V	1024	8 pin DIP

MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature (2)	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation (2)	535mW@T_A>70°C
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+0.3V to −20V

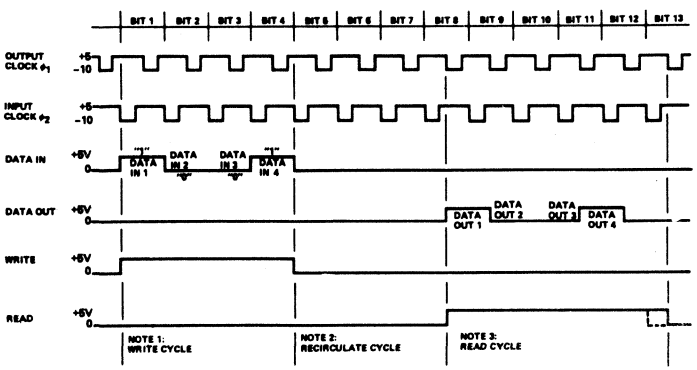
NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. All inputs are protected against static charge.
4. See "Minimum Operating Frequency" graph for low limits on data rep. rate.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserving the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. Parameters are valid over operating temperature range unless otherwise specified.
9. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are V_{IH} = V_{CC} - 1.85V and V_{IL} = V_{CC} - 4.15V.
10. V_{OL} is a function of the input characteristics of the driven TTL/DTL gate I_{OI} and V_{CLAMP} and the value of the pull-down resistor (R_L).

DC CHARACTERISTICS T_A = 0°C to +70°C; V_{CC} = +5V ±5%; V_{DD} = −5V ±5% unless otherwise noted.

SYMBOL	TEST	MIN	TYPICAL	MAX	UNIT	CONDITION
I_{LI}	Input Load Current		10	500	nA	V_{IN} =-5.5V; T_A = 25°C
I_{LO}	Output Leakage Current		10	1000	nA	$V_{\phi1}$ = $V_{\phi2}$ = -12V; V_{DD} = -5 V_{OUT} =-5.5V; T_A = 25°C
I_{LC}	Clock Leakage Current		10	1000	nA	V_{ILC} = -12V ; T_A = 25°C
I_{DD}	Power Supply Current: 2524		15	35	mA	Continuous Operation; ϕpW = 150nS; f = 1 MHz
	2525		25	35	mA	V_{ILC} = -12V; T_A = 25°C V_{DD} = -5.5V
V_{IL}	Input "Low" Voltage	-5.0		+0.6	V	Note 9
V_{IH}	Input "High" Voltage	+3.4		5.3	V	Note 9
V_{ILC}	Clock Input "Low" Voltage	-12.0		-10.0	V	
V_{IHC}	Clock Input "High" Voltage	4.0		5.3	V	

EXAMPLE TIMING DIAGRAM



NOTE:
This is a simplified illustration of the timing of a 4 bit recirculating shift register showing the 3 basic modes of operation.

NOTE 1: (WRITE cycle)

The positive and negative going edge of the "Write" control is coincident with the negative going edge of the input clock (ϕ_2). The "Read" control may be either "1" or "0".

NOTE 2: (RECIRCULATE cycle)

Data recirculates if the "Write" control line is "0". "Read" may be either "1" or "0".

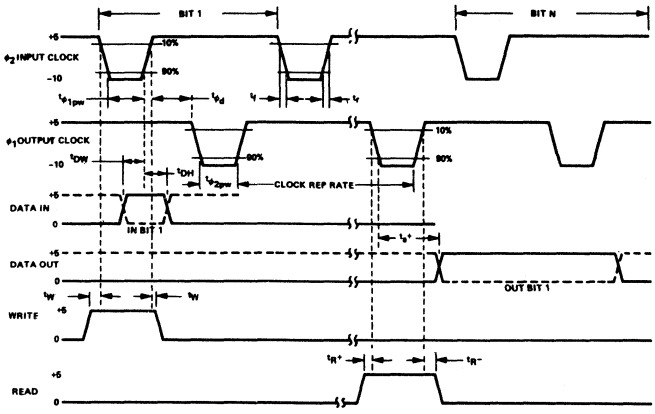
NOTE 3: (READ cycle)

The positive going edge of the "Read" control is coincident with the negative edge of the output clock (ϕ_1). The negative going edge of "Read" is coincident with the negative going edge of either clock pulse succeeding the last desired data output bit. "Write" may be either "1" or "0".

CONDITIONS OF TEST

Input rise and fall times: 10 sec Output load is 1 TTL gate

TIMING DIAGRAM



NOTE:

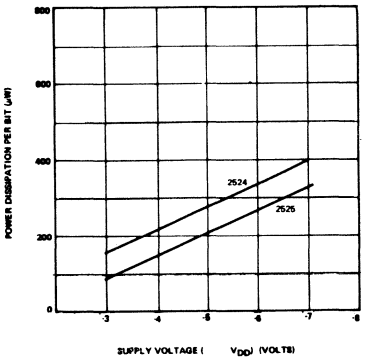
1. N = 512 for 2524 N= 1024 for 2525
2. Note that the Read Input is AND'ed with $\overline{\phi}_1$; therefore this function is not valid until ϕ_1 occurs.

AC CHARACTERISTICS $T_A = +25^\circ C$ $V_{CC} = +5V \pm 5\%$; $V_{DD} = -5V \pm 5\%$; $V_{ILC} = -11V$

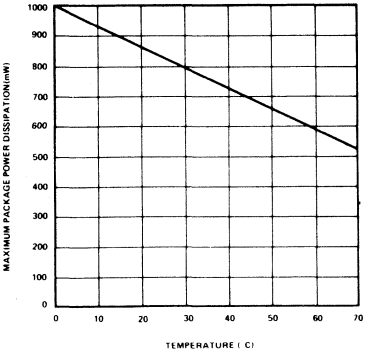
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
Frequency	Clock Data Rep Rate	.0005 (Note 4)	5	3	MHz	$W = R = V_{CC}$
$t_{\phi pw}$	Clock Pulse Width	135	85		ns	
$t_{\phi d}$	Clock Pulse Delay	10			ns	
t_r;t_f	Clock Pulse Transition	10		1000	ns	
t_{DW}	Data Write (Setup) Time	70			ns	
t_{DH}	Data to Clock Hold Time	20			ns	
t_{a+}	Clock to Data Out Delay			100	ns	
t_{R-}; t_{W-}	Clock to "Read" or "Write" Timing	0			ns	
t_{R-}; t_{W+}	Clock to "Read" or "Write" Timing	0			ns	
C_{in}	Input Capacitance			5	pF	1MHz; $V_I = V_{CC}$; $V_{AC} = 25m\ V_{P-P}$
C_{out}	Output Capacitance			5	pF	1MHz; $V_0 = V_{CC}$; $V_{AC} = 25m\ V_{P-P}$
C_ϕ	Clock Capacitance 2524 2525			 80 160	 pF pF	1MHz; $V = V_{CC}$; $V_{AC} = 25m\ V_{P-P}$
V_{OL}	Output "Low" Voltage		-1.0		V	$R_L = 3.0K$; 1 TTL Load (I_L = 1.6mA) Note 10
V_{OH1}	Output "High" Voltage Driving 1 TTL Load	2.4	3.5		V	$R_L = 3.0K$; 1 TTL Load ($I_L = 100\mu A$)
V_{OH2}	Output "High" Voltage Driving MOS	3.6	4.0		V	$R_L = 5.6K$; $C_L = 10pF$

CHARACTERISTIC CURVES

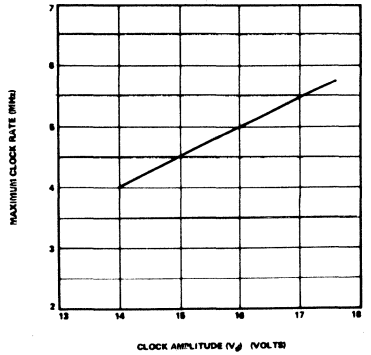
POWER DISSIPATION/BIT VERSUS SUPPLY VOLTAGE



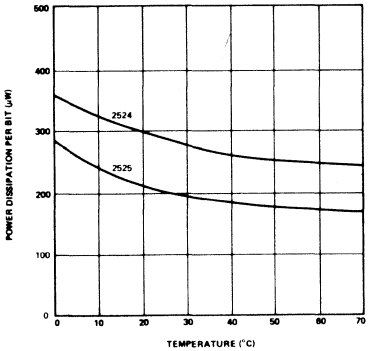
MAXIMUM PACKAGE POWER DISSIPATION VERSUS TEMPERATURE



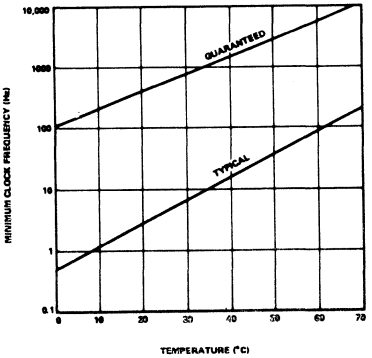
MAXIMUM CLOCK RATE VERSUS CLOCK AMPLITUDE



POWER DISSIPATION/BIT VERSUS TEMPERATURE



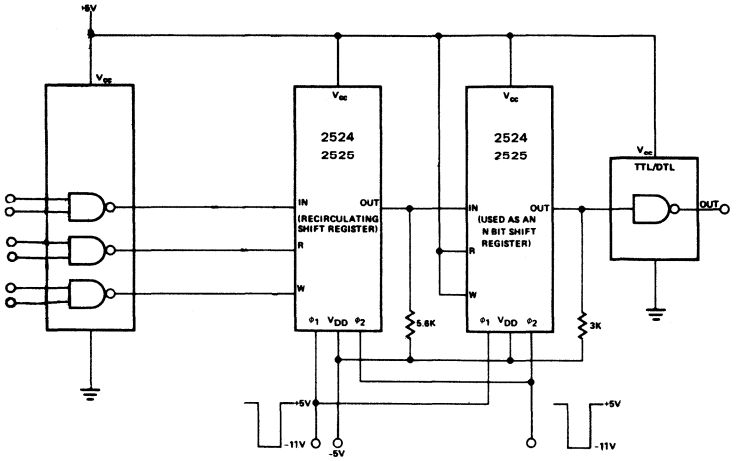
MINIMUM OPERATING CLOCK FREQUENCY VERSUS TEMPERATURE



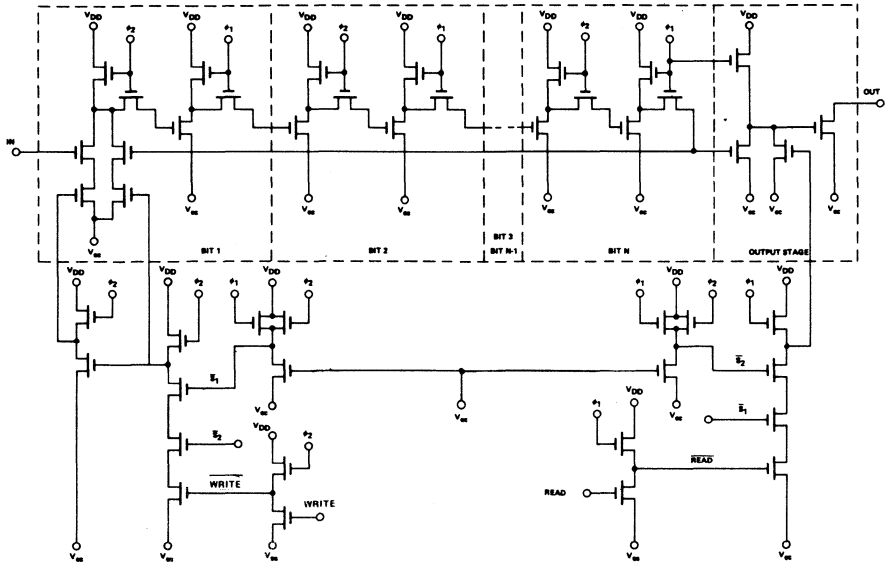
NOTE:
Conditions for typical curves: V_{CC} = +5V, V_{DD} = -5V, clock duty cycle = 35%, f_{CLK} = 3MHz, $V\phi_{p\text{-}p}$ = 16V, $\phi_{PW1} = \phi_{PW2}$ = 80ns, T_A = +25°C unless otherwise noted.

APPLICATIONS DATA

TTL/DTL/MOS INTERFACES



CIRCUIT SCHEMATIC



NOTE
N = 512 for 2524
N = 1024 for 2525

signetics

DUAL 256-250-240 BIT STATIC SHIFT REGISTERS

SILICON GATE 2500 SERIES

2527
2528
2529

DESCRIPTION

The Signetics 2500 Series Dual 256, 250 and 240 bit recirculating static shift registers consist of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip.

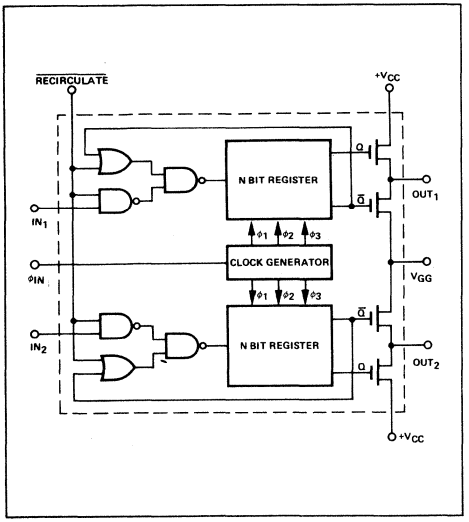
FEATURES

- PUSH-PULL OUTPUTS
- TTL/DTL COMPATIBLE CLOCK – PROVIDES EXTREMELY LOW CLOCK CAPACITANCE
- RECIRCULATION PATH ON CHIP
- THREE BIT LENGTHS AVAILABLE
- HIGH FREQUENCY OPERATION – 3 MHz TYPICAL CLOCK & DATA RATE
- TTL, DTL COMPATIBLE INPUTS AND OUTPUTS
- STANDARD PACKAGE – 8 LEAD SILICONE DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST STATIC BUFFER MEMORIES
CRT REFRESH MEMORIES – LINE STORAGE
DELAY LINES
CASSETTE RECORDERS

BLOCK DIAGRAM

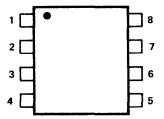


BIPOLAR COMPATIBILITY

The clock and signal inputs of these registers can be driven directly by standard bipolar integrated (TTL, DTL, etc.) or by MOS circuits. The outputs drive directly into TTL/DTL without requiring external resistors.

PIN CONFIGURATION (Top View)

V PACKAGE



1. $\overline{\text{Recirculate}}$
2. IN_1
3. OUT_1
4. V_{GG}
8. V_{CC}
7. IN_2
6. OUT_2
5. ϕ_{IN}

TRUTH TABLE

$\overline{\text{RECIRCULATE}}$	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is Written
1	1	"1" is Written

NOTE: "0" = 0V; "1" = +5V

PART IDENTIFICATION TABLE

PART NUMBER	BIT LENGTH	PACKAGE
2527V	Dual 256	8 Pin DIP
2528V	Dual 250	8 Pin DIP
2529V	Dual 240	8 Pin DIP

MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature (2)	0°C to +70°C
Storage Temperature	-65°C to +150°C
Package Power Dissipation at T_A = 70°C	535 mW
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+0.3V to -20V

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH}, and V_{OH} which are stated for a V_{CC} of exactly 5 volts.

DC CHARACTERISTICS T_A = 0°C to +70°C; V_{CC} = +5V(8); V_{GG} = -12V ±5% unless otherwise noted.

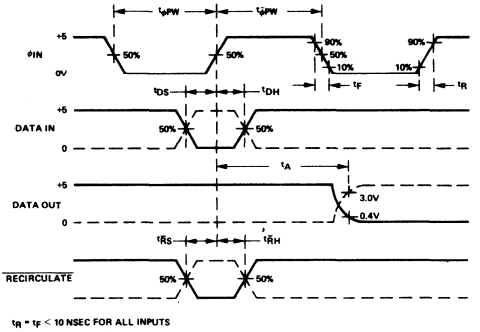
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} = 5.5V, T_A = 25°C
I_{LC}	Clock Leakage Current		10	500	nA	V_{ILC} = 0V, T_A = 25°C
I_{GG}	Power Supply Current		28	35	mA	Continuous Operation F = 2.5 MHz, T_A = 25°C Outputs Open
V_{IL}	Input "Low" Voltage			1.05	V	
V_{IH}	Input "High" Voltage	3.2		5.3	V	
V_{ILC}	Clock Input "Low" Voltage			1.05	V	
V_{IHC}	Clock Input "High" Voltage	3.2		5.3	V	

AC CHARACTERISTICS T_A =0° to +70°C, V_{CC} = +5V(8); V_{GG} = -12V +5%, V_{IC} = 0,4 to 4.0V

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
FREQUENCY	Clock Rep Rate	DC	2.5	1.5	MHz	See Maximum Frequency Curve
$t_{\phi PW}$	Clock Pulse Width	0.2	0.1	100	μs	
$t_{\overline{\phi} PW}$	$\overline{\text{Clock}}$ Pulse Width	0.2		DC	μs	
t_R t_F	Clock Pulse Transition			1	μs	
t_{DS}	Data Set-up Time	50			ns	
t_{DH}	Data Hold Time	50			ns	
t_A	Clock to Data Out Delay		330	450	ns	I_{OL} = 1.6mA
$t_{\overline{R}S}$	$\overline{\text{Recirculate}}$ Set-up Time	50			ns	
$t_{\overline{R}H}$	$\overline{\text{Recirculate}}$ Hold Time	50			ns	
C_{IN}	Input Capacitance			5	pF	@ 1 MHz; V_{IN} = V_{CC}; V_{AC} = 25mV p-p
C_ϕ	Clock Capacitance			5	pF	@ 1 MHz; V_ϕ = V_{CC}; V_{AC} = 25mV p-p
V_{OL}	Output "Low" Voltage			0.4	V	1 TTL load (I_L = 1.6mA)
V_{OH1}	Output "High" Voltage Driving 1 TTL Load	3.0	3.5		V	1 TTL load (I_I = 100μA)
V_{OH2}	Output "High" Voltage Driving MOS	3.5	4.0		V	

CONDITIONS OF TEST Input rise and fall times: 10 nsec. Output load is 1 TTL gate.

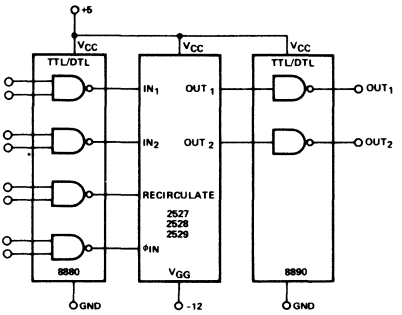
TIMING DIAGRAM



$t_R = t_F < 10$ NSEC FOR ALL INPUTS

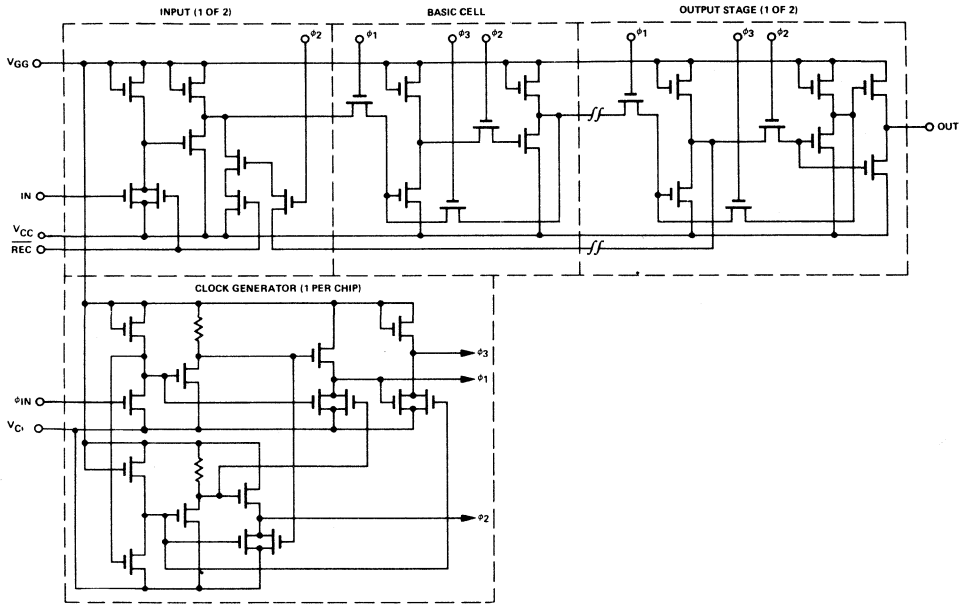
APPLICATIONS INFORMATION

TTL/DTL/MOS INTERFACES

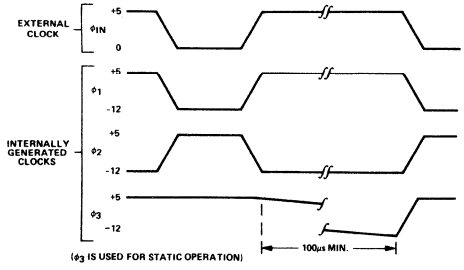


Note: When using 7400 series data, recirculate and clock drivers, connect 10k resistor from driver output to V_{CC}. This insures an adequate "1" level input for the MOS register. See page 13 of MOS Handbook.

SCHEMATIC DIAGRAM

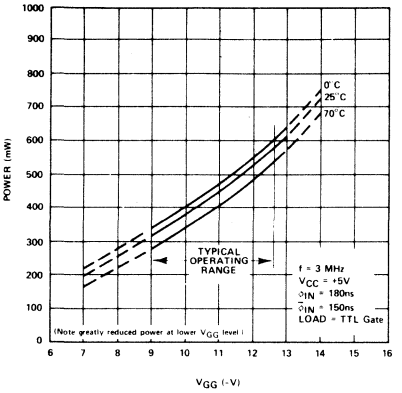


CLOCKING WAVEFORMS

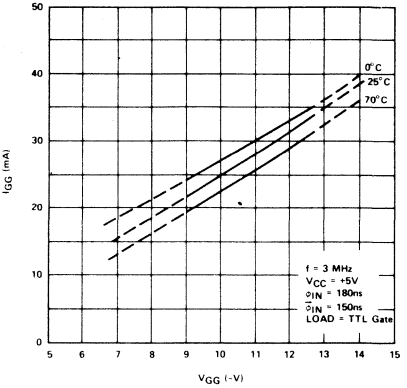


CHARACTERISTIC CURVES

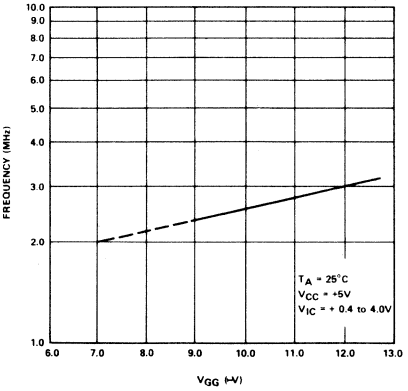
POWER DISSIPATION VS SUPPLY VOLTAGE



SUPPLY CURRENT VS SUPPLY VOLTAGE

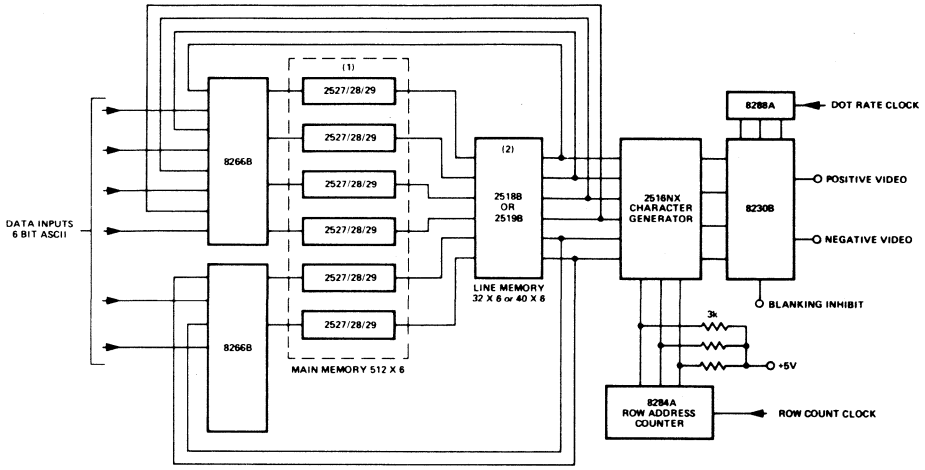


TYPICAL DATA RATE VS SUPPLY VOLTAGE



APPLICATIONS INFORMATION (Cont'd)

12 LINE, 32 OR 40 CHARACTER PER LINE CRT DISPLAY MEMORY SYSTEM



(1) Duals connected in series.
(2) These registers include internal recirculate. Two 8266B multiplexers are used for system recirculate.

signetics

QUAD 80-BIT STATIC SHIFT REGISTER | 2532

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The Signetics 2532 Static Shift Register consists of enhancement mode P-Channel silicon gate MOS devices integrated on a single monolithic chip. Each of the four 80-bit registers is provided with an independent input, push-pull output and recirculation control. The single phase clock is common to all four registers. All inputs and outputs including the clock interface directly with TTL or DTL circuits without external components.

Data is entered when the clock is at a logic "1". Data is shifted when the clock goes low. When the Recirculate control is at a logic "1", data recirculates and is continuously available at the output, data input is inhibited. With the Recirculate control is at a logic "0", data is entered.

FEATURES

- TOTAL TTL COMPATIBILITY
- SINGLE CLOCK LINE
- RECIRCULATE PATH ON CHIP
- DC TO 1.5 MHz OPERATION GUARANTEED
- LOW POWER (TYPICALLY 400 μW/BIT)
- PIN-FOR-PIN REPLACEMENT FOR (DYNAMIC) MK1007P AND TMS3409
- POWER SUPPLIES +5V AND −12V

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST STATIC BUFFER MEMORIES
CRT REFRESH MEMORIES – LINE STORAGE
DELAY LINES
DIGITAL FILTERING

SPECIAL FEATURES

The three clock phases used by the static register cells are generated internally by an on-chip generator. This clock generator is controlled by a single TTL/DTL logic level input.

BIPOLAR COMPATIBILITY

All inputs of these registers, including the clock can be driven directly by bipolar TTL/DTL integrated circuits without external components. Outputs are push-pull operating between 0V and +5V and provide a sink current of 1.6mA for a fanout of one TTL load.

PART IDENTIFICATION

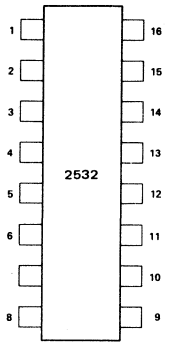
PART NUMBER	BIT LENGTH	PACKAGE
2532B	Quad 80	16-Pin DIP

MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature (2)	0°C to +70°C
Storage Temperature	-65°C to +150°C
Package Power Dissipation at T_A = 70°C	640 mW
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+0.3V to -20V

PIN CONFIGURATION (Top View)

B PACKAGE



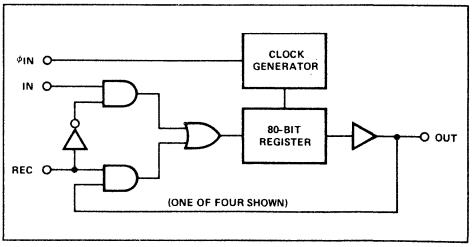
1.	OUT 1	16.	V_{CC}
2.	Recirculate 1	15.	IN 4
3.	IN 1	14.	Recirculate 4
4.	OUT 2	13.	OUT 4
5.	Recirculate 2	12.	V_{GG}
6.	IN 2	11.	ϕ IN
7.	OUT 3	10.	IN 3
8.	V_{DD} (Ground)	9.	Recirculate 3

TRUTH TABLE

RECIRCULATE	INPUT	FUNCTION
0	0	"0" is Written
0	1	"1" is Written
1	0	Recirculate
1	1	Recirculate

NOTE: "0" = 0V, "1" = +5V

BLOCK DIAGRAM



DC CHARACTERISTICS T_A = 0°C to +70°C; V_{CC} = +5V ±5%; V_{GG} = −12V ±5% unless otherwise noted.

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} = 5.5V, T_A = 25°C
I_{LC}	Clock Leakage Current		10	500	nA	V_{ILC} = 0V, T_A = 25°C
I_{GG}	Power Supply Current		6	10	mA	Continuous Operation F = 1.5 MHz, T_A = 25°C Outputs Open
I_{CC}	Power Supply Current		12	20	mA	
V_{IL}	Input "Low" Voltage			+0.6	V	Note 8
V_{IH}	Input "High" Voltage	+3.4		5.3	V	Note 8
V_{ILC}	Clock Input "Low" Voltage			+0.6	V	Note 8
V_{IHC}	Clock Input "High" Voltage	+3.4		5.3	V	Note 8

AC CHARACTERISTICS T_A = 0°C to 70°C; V_{CC} = +5V ±5%; V_{GG} = −12V ±5%.

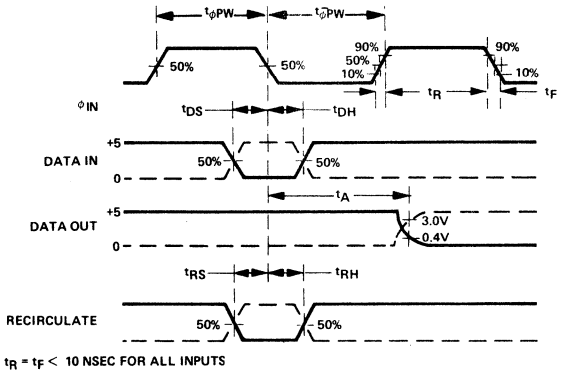
(CONDITIONS OF TEST Input rise and fall times: 10 nsec. Output load is 1 TTL Gate.)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
Frequency	Clock Rep Rate	DC	3.0	1.5	MHz	
$t_{\phi}PW$	Clock Pulse Width	0.33		100	μs	See Timing Diagram note
$t_{\bar{\phi}}PW$	$\overline{\text{Clock}}$ Pulse Width	0.33		DC	μs	
t_R,t_F	Clock Pulse Transition			5	μs	
t_{DS}	Data Set-up Time	120			ns	
t_{DH}	Data Hold Time	0			ns	
t_A	Clock to Data Out Delay			400	ns	I_{OL} = 1.6mA
t_{RS}	Recirculate Set-up Time	150			ns	
t_{RH}	Recirculate Hold Time	0			ns	
C_{IN}	Input Capacitance			5	pF	@ 1 MHz; V_{IN} = V_{CC}; V_{AC} = 25mV p-p
C_{ϕ}	Clock Capacitance			5	pF	@ 1 MHz; V_{ϕ} = V_{CC}; V_{AC} = 25mV p-p
V_{OL}	Output "Low" Voltage			+0.5	V	I_{OL} = 1.6mA
V_{OH}	Output "High" Voltage	+3.8			V	I_{OH} = 100μA

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 125°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are V_{IH} = V_{CC} - 1.85V and V_{IL} = V_{CC} - 4.15V.

TIMING DIAGRAM

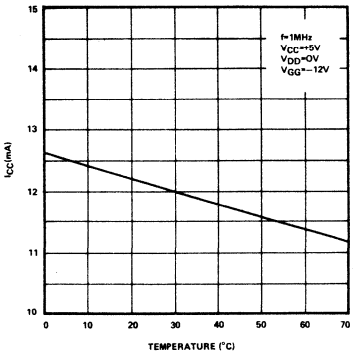


$t_R = t_F <$ 10 NSEC FOR ALL INPUTS

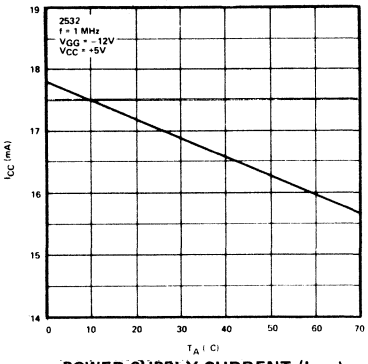
NOTE: CLOCK MUST BE STOPPED IN THE TTL "0" STATE TO RETAIN DATA DURING STATIC OPERATION.

TYPICAL CHARACTERISTIC CURVES

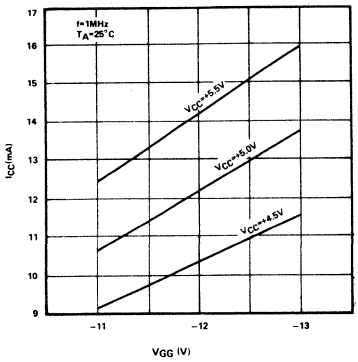
POWER SUPPLY CURRENT (I_{CC}) VERSUS TEMPERATURE



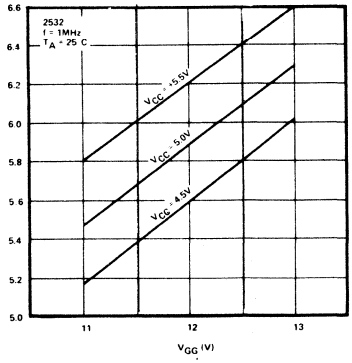
POWER SUPPLY CURRENT (I_{CC}) VERSUS TEMPERATURE



POWER SUPPLY CURRENT (I_{CC}) VERSUS POWER SUPPLY VOLTAGE (V_{GG})

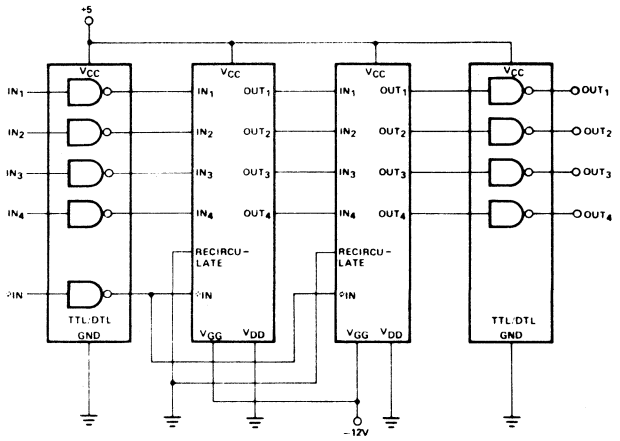


POWER SUPPLY CURRENT (I_{GG}) VERSUS POWER SUPPLY VOLTAGE (V_{GG})

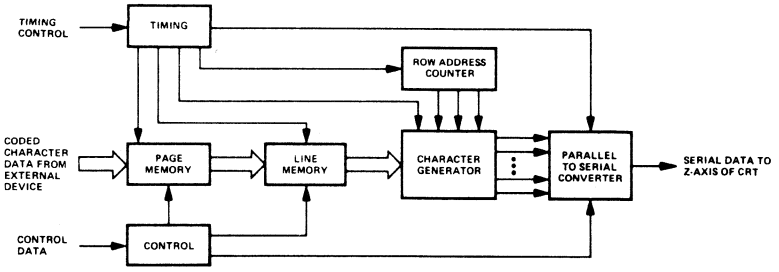


APPLICATIONS INFORMATION

DTL/TTL – MOS – MOS – DTL/TTL INTERFACING



NOTE: All unused inputs must be tied to a "1" or a "0", i.e., MOS inputs cannot be left floating.



PAGE MEMORY: THIS MEMORY CONTAINS CHARACTER CODES. TYPICALLY, IT CONTAINS THE SAME NUMBER OF CHARACTER CODES AS THE NUMBER OF CHARACTER ON A FULL SCREEN.

LINE MEMORY: THIS MEMORY CONTAINS THE CHARACTER CODES FOR ONE LINE OF THE CRT DISPLAY.

CHARACTER GENERATOR: THE CHARACTER GENERATOR IS TYPICALLY A ROM WHICH CONVERTS CHARACTER CODE INPUTS TO DOT MATRIX BITS AT THE OUTPUT.

NOTE: THE 2532 IS VERY WELL SUITED FOR USE AS A LINE MEMORY.

signetics

1024-BIT STATIC SHIFT REGISTER | 2533

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The Signetics 2533 Static Shift Register consists of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip.

The 1024-bit register is equipped with two data inputs together with a "Stream Select" control to facilitate external recirculation.

The single phase clock input, data input, data output, and stream select control will interface directly with TTL/DTL circuits without external components.

Data is entered when the clock is at a logic "1". Data is shifted when the clock goes low.

FEATURES

- TOTAL TTL COMPATIBILITY
- SINGLE CLOCK LINE
- DC TO 1.5MHz GUARANTEED
- LOW POWER (TYPICALLY 250μW/BIT)
- POWER SUPPLIES +5V AND −12V
- 8-PIN DIP
- STREAM SELECT FOR EASY RECIRCULATION

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST STATIC BUFFER MEMORIES
CRT REFRESH – PAGE MEMORY
DELAY LINES
DRUM MEMORY REPLACEMENT

SPECIAL FEATURES

The three clock phases used in the static register cells are generated internally by an on-chip generator. This clock generator is controlled by a single TTL/DTL logic level input.

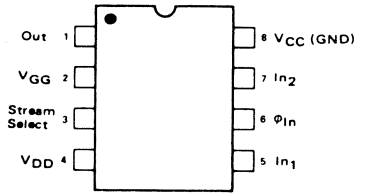
Recirculation of data in the 2533 is accomplished by simply jumpering the output back to In 2. The stream select control then becomes a Data Entry/Recirculate Control.

BIPOLAR COMPATIBILITY

All inputs of this register, including the clock, can be driven directly by bipolar TTL/DTL integrated circuits without external components. The output is push-pull, operating between 0V and +5V, and provides a sink current of 1.6mA for a fanout of one TTL load.

PIN CONFIGURATION (Top View)

"V" PACKAGE

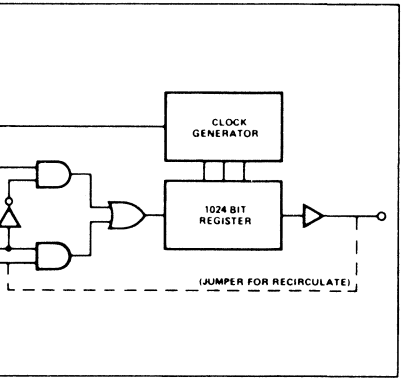


TRUTH TABLE

STREAM SELECT	FUNCTION
0	IN 1 SELECTED
1	IN 2 SELECTED

NOTE: "0" = 0V, "1" = +5V

BLOCK DIAGRAM



PART IDENTIFICATION TABLE

PART NUMBER	BIT LENGTH	PACKAGE
2533 V	1024	8-Pin DIP

MAXIMUM GUARANTEED RATINGS(1)

Operating Ambient Temperature(2)	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation (Note 2)	535mW @ T_A >25°C
Data and Clock Input Voltages and Supply Voltages with Respect to V_{CC}	+0.3V to −20V

DC CHARACTERISTICS

(T_A = 0°C to +70°C; V_{CC} = +5V ±5%; V_{GG} = −12V ±5% unless otherwise noted.)

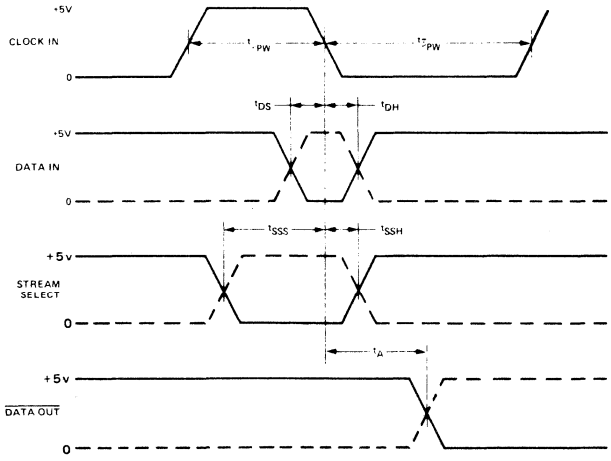
SYMBOL	TEST	MIN.	TYP.	MAX.	UNITS	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} = 0, T_A = 25°C
I_{LC}	Clock Leakage Current		10	500	nA	V_{ILC} = GND, T_A = 25°C
I_{CC}	Power Supply Current		16	30	mA	Continuous Operation
I_{GG}	Power Supply Current		5.0	7.5	mA	F = 1.5MHz
V_{IL}	Input "Low" Voltage			+0.6	V	V_{CC} = +5V
V_{IH}	Input "High" Voltage	+3.4		5.3	V	V_{CC} = +5V
V_{ILC}	Clock Input "Low" Voltage			+0.6	V	V_{CC} = +5V
V_{IHC}	Clock Input "High" Voltage	+3.4		5.3	V	V_{CC} = +5V

Note 8

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated corresponding to a thermal resistance of 150 C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25 C and nominal supply voltages.
8. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0 C to +70 C. Actual input requirements with respect to V_{CC} are V_{IH} V_{CC} 1.85V and V_{IL} V_{CC} 4.15V.

TIMING DIAGRAM



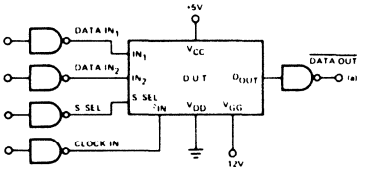
NOTE: A TIMES MEASURED AT 50% POINTS WITH INPUT tr, tf ≤ 10ns.

B CLOCK MUST BE STOPPED IN TTL "0" STATE TO RETAIN DATA DURING STATIC MODE OPERATION.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = +5V ±5%; V_{GG} = −12V ±5%).

SYMBOL	TEST	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Frequency	Clock & Data Rep Rate		2	1.5	MHz	
$t_{\phi PW}$	Clock Pulse Width	.350		100	μs	See Timing Diagram Note
$t_{\overline{\phi}PW}$	Clock Pulse Width	250			ns	
t_r, t_f	Clock Pulse Transition			1	μs	
t_{DW}	Data Write Set-Up Time	50			ns	
t_{DH}	Data to Clock Hold Time	50			ns	
t_A	Clock to Data Out Delay		200	300	ns	
t_{SSH}	Stream Select Hold Time	50			ns	
t_{SSS}	Stream Select Set-Up Time	80			ns	
C_{IN}	Input Capacitance			5	pF	@ 1 MHz, $V_{IN} = V_{CC}$ V_{AC} = 25mV p-p
C_{OUT}	Output Capacitance			5	pF	@ 1 MHz, $V_{OUT} = V_{CC}$ V_{AC} = 25mV p-p
C_ϕ	Clock Capacitance			5	pF	@ 1 MHz, $V_\phi = V_{CC}$ V_{AC} = 25mV p-p
V_{OL}	Output "Low" Voltage			+0.5	V	I_{OL} = 1.6mA
V_{OH}	Output "High" Voltage	+3.8			V	I_{OH} = 100μA

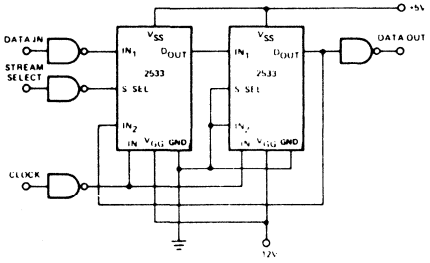
A.C. TEST SETUP



NOTES:
Measure t_A between device input and point (a).
Gates are standard 7400.

APPLICATIONS INFORMATION

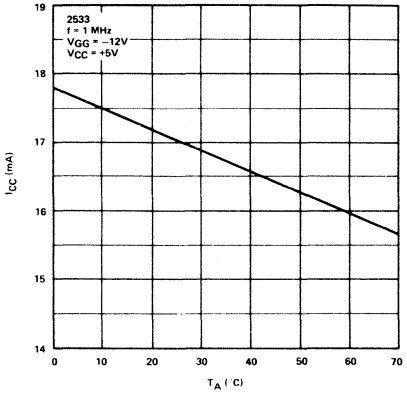
2048-BIT STORAGE REGISTER WITH RECIRCULATE



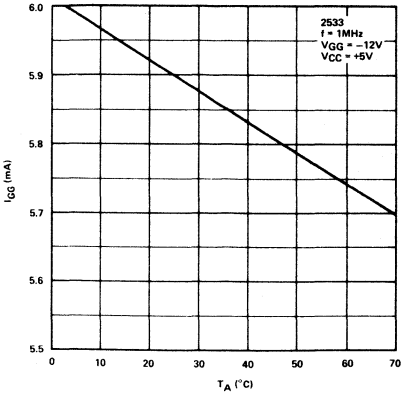
NOTE:
Gates are standard DTL or TTL.

TYPICAL CHARACTERISTIC CURVES

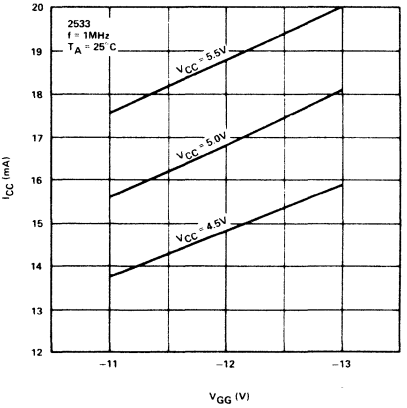
POWER SUPPLY CURRENT (I_{CC}) VERSUS TEMPERATURE



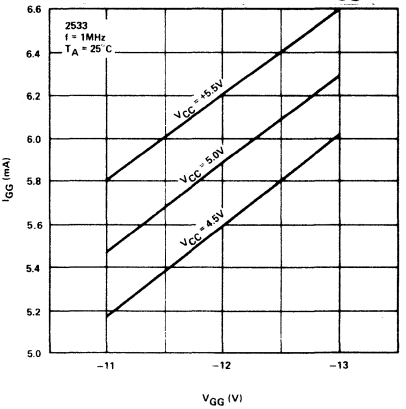
POWER SUPPLY CURRENT (I_{GG}) VERSUS TEMPERATURE



POWER SUPPLY CURRENT (I_{CC}) VERSUS POWER SUPPLY VOLTAGE (V_{GG})



POWER SUPPLY CURRENT (I_{GG}) VERSUS POWER SUPPLY VOLTAGE (V_{GG})



SIGNETICS INTERNATIONAL CORPORATION

EUROPEAN HEADQUARTERS

Signetics International Corporation
Yeoman House
63 Croydon Road
Penge
London SE20 7TW
England
Telephone: 01-659 2111
Telex: 946619

SALES OFFICES

FRANCE

Signetics S A R L
F92100 Boulogne
36 Rue de Silly
Telephone: 604-8127
Telex: 26801

SCANDINAVIA

Signetics AB
Vretenvägen 2
17154 Solna
Stockholm
Telephone: (08) 29-31-00/29-95-95
Telex: 13155

UNITED KINGDOM

Signetics International Corporation
Yeoman House
63 Croydon Road
Penge
London SE20 7TW
Telephone: 01-659 2111
Telex: 946619

WEST GERMANY

Signetics G m b H
D-4006 Dusseldorf-Erkrath
Rathelbeckerweg 42
Telephone: (0211) 244238
Telex: 8588514

Signetics G m b H
(German sales headquarters)
D-8 München 19
Dantestrasse 29
Telephone: (089) 15-20-20/
15-20-29

Signetics G m b H
D-7 Stuttgart 80
Ernsthaldenstrasse 17
Telephone (0711) 73-50-61
Telex: 7255798

EUROPEAN MANUFACTURING PLANTS

GERMANY

Signetics G m b H
D 8960 Nördlingen
Oettingerstrasse 6
Telephone: (09081) 6001
Telex: 51709

PORTUGAL

Electronica
Signetics de Portugal LDA
Estrada de Santas - Manteigadas
Setubal
Telephone: 28001
Telex: 16250

UNITED KINGDOM

Signetics International Corporation
Preston Road
Linlithgow
West Lothian
Scotland
Telephone: 050-684 3161/4511
Telex: 72625

STOCKING DISTRIBUTORS

AUSTRIA

Ing. Ernst Steiner
A-1130 WIEN
Geylinggasse 16
Telephone: (0222) 822674
Telex: 74013

BELGIUM/BELGIQUE

Ritro Electronics S.A.
156 Mechelsesteenweg
Chaussee de Maline
2000 Antwerpen
Anvers
Telephone: (31) 37-22-68
Telex: 33637

FINLAND

AB Kuno Kallman OY
Nuijamiestentie 5C
00400 Helsinki 40
Telephone: 575231/575362
Telex: 123162

FRANCE

CESIME
18 Place de France
95200 Sarcelles
Telephone: 990 56 23
Telex: none

ELIC
8-10 Avenue de Grand Sablon
38 La Tronche
Telephone: 76 87-67-71
Telex: 32739

Fadico
13 Cours de Chazelles
56100 Lorient
Telephone: (97) 21-42-96
Telex: none

REA Distribution
57 Rue Henry Litolff
92270 Bois Colombes
Telephone: 784 71 19
Telex: 63694

RTF
73 Avenue Charles de Gaulle
92200 Neuilly Sur Seine
Telephone: 722-70-40
Telex: 65933

ITALY

Metroelettronica S A S
Viale Cirene 18
1-20135 Milano
Telephone: 546-26-41
Telex: 33168

MESA S.P.A.
Via Canova 21
20145 Milano
Telephone: 02-349 10 40
Telex: 32250

NETHERLANDS

Ritro Electronics B.V.
Postbus 123
Prins Hendrikweg 19
Barneveld
Telephone: (03420) 5041
Telex: 40553

NORWAY

A S Kjell Bakke
Kjellergt 11
Lillestrøm 2000
Telephone: 71-18-72/71-53-30
Telex: 19407

SOUTH AFRICA

Allied Electric (Pty) Limited
P.O. Box 6090
Dunswart
Transvaal
Telephone: Johannesburg
52-4341
Telex: 437823

SPAIN

Ataio Ingenieros S.A.
Enrique Larreta 10Y12
Madrid 16
Telephone: 215-3543/733-0562
Telex: 27249

Instrumentos Electronicos de Precision SA
Alcalde Sainz de Baranda, 33
Madrid 9
Telephone: 274 10 07
Telex: 22961

SWEDEN

AB Kuno Källman
Folkungagatan 16-18
41102 Gothenburg
Telephone: 80-30-20
Telex: 21072

AB Kuno Källman
Sibyllegatan 28
11443 Stockholm
Telephone: (08) 67-17-11/
67-15-95
Telex: 17165

SWITZERLAND

Omni Ray AG
Dufourstrasse 56
8008 Zurich
Telephone: (01) 34-07-66
Telex: 53239

WEST GERMANY

Distron G m b H
D-1 Berlin 33
Mecklenburgische Strasse 24b
Telephone: (030) 82-33-064/5
Telex: 182758

EBV - Elektronik G m b H
D-4 Dusseldorf
Oststrasse 129
Telephone: (0211) 84-84-6/7
Telex: 8587267

EBV - Elektronik G m b H
D-6 Frankfurt
Myliusstrasse 54
Telephone: (0611) 72-04-16/18
Telex: 413590

EBV - Elektronik G m b H
D-8 München 90
Gabriel-Max-Strasse 72
Telephone: (089) 64-40-55/58
Telex: 524535

EBV - Elektronik G m b H
D-7 Stuttgart 1
Alexanderstrasse 63
Telephone (0711) 24-74-81
Telex: 722271

Mirotronic
2 Hamburg 20
Christian Foerster Strasse 7
Telephone: 040 491 10 14
Telex: 215427

Mütron - Müller & Co KG
D-28 Bremen 1
Bornstrasse 22
Telephone: (0421) 31-04-85
Telex: 245325

Electis Ruggaber KG
7250 Leonberg
Hertichstrasse 41
Telephone: 07152/7081
Telex: 724192

UNITED KINGDOM

A M Lock & Co Limited
Neville Street
Middleton Road
Oldham
Lancs
OL9 6LF
Telephone: (061) 652 0434
Telex: 669971

Apex Components Limited
396 Bath Road
Slough, Bucks
Telephone: Burnham (06286) 63741
Telex: 848519

Quarndon Electronics Limited
Slack Lane
Derby
Derbyshire
DE3 3ED
Telephone: (0332) 32651
Telex: 37163

SDS (Components) Limited
Hilsea Industrial Estate
Portsmouth
Hants
PO3 5JW
Telephone: (0705) 65311
Telex: 86114

Semicomps Limited
5 Northfield Industrial Estate
Beresford Avenue
Wembley, Middlesex
HA0 1SD
Telephone: 01-903 3161
Telex: 935243

Semicomps Northern Limited
East Bowmont Street
Kelso
Roxburghshire
Scotland
Telephone: Kelso 2366
Telex: 72692

Semicomps Limited
North Midlands Division
Ingrow Lane
Keighley
West Yorkshire
BD21 5HR
Telephone: (05352) 65191
Telex: 517343

STOCKING REPRESENTATIVES

FINLAND

AB Kuno Källman OY
Nuijamiestentie 5C
00400 Helsinki 40
Telephone: 575231/575362
Telex: 123162

SWEDEN

AB Kuno Källman
Folkungagatan 16-18
41102 Gothenburg
Telephone: 80-30-20
Telex: 21072

AB Kuno Källman
Sibyllegatan 28
11443 Stockholm
Telephone: (08) 67-17-11/ 67-15-95
Telex: 17165

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Omni Ray AG
Dufourstrasse 56
8008 Zurich
Telephone: (01) 34-07-66
Telex: 53239